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Design and Implementation of 3 kW All-SiC Current Source Inverter

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Abstract: In this paper, the optimal design and implementation of a silicon-carbide (SiC) power semiconductor-based current source inverter (CSI) with a power rating of 3 kW focusing on high power density are discussed in detail. The proposed methodology integrates analytical and numerical techniques to optimize the design of passive components, including filter capacitors and the DC-link inductor, and provides a comprehensive analysis of power semiconductor losses. The losses in the DC-link inductor as well as in the output capacitor are strongly dependent on the modulation strategy. Semi-analytical loss models are therefore derived for the most advanced modulation strategy, which are subsequently used to increase volumetric power density. The theoretical findings are experimentally validated using an ultra-compact, high-efficiency 3 kW three-phase CSI prototype operating at up to 100 kHz switching frequency. The experimental results confirm the efficiency of the proposed design and demonstrate its potential for high-power, compact drive applications.

Keywords: current source inverter; wide-bandgap semiconductor; three-phase converter

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1. Introduction

The adoption of wide-bandgap (WBG) semiconductor switches, such as silicon carbide (SiC) and gallium nitride (GaN), has enabled a substantial increase in the switching frequencies of power electronic converters used in electric drives. These advanced devices not only offer lower conduction losses but also demonstrate superior performance in high-temperature environments [1,2]. However, when WBG devices are used in voltage-source inverters (VSIs), e.g., the two-level six-switch inverter, very fast switching transients can be implemented resulting in high $\mathrm{d}v/\mathrm{d}t$. These high switching transients introduce challenges such as elevated electromagnetic interference (EMI), overvoltages at motor terminals in the case of long motor cables, increased bearing currents, and additional losses in the electric machine [3]. A sinus motor filter connected to the inverter output terminals could help to mitigate the introduced transients, but adds extra volume, cost, and complexity and leads to increased losses and reduced power density.

A promising alternative to the conventional VSI with its limitation is the application of a current source inverter (CSI) topology, as discussed in [3–5]. The CSI inherently filters the output quantities, i.e., inverter output voltages and output currents, mitigating the negative effects of high switching frequencies. Comparisons of the pros and cons of the VSI and CSI topology have already been extensively covered in [6–8]. Figure 1 shows the basic structure of a three-phase CSI supplied by a buck-stage from a DC voltage source. The DC-link inductor, L_{dc}, is split between the positive and negative DC-rails and serves as the primary energy storage element. By appropriately controlling the buck-stage, the DC-link current,

i_{dc}, is maintained at a nearly constant value. Using pulse-width modulation (PWM) in the inverter stage, this constant DC current is then shaped into arbitrary three-phase current waveforms, i_a, i_b, and i_c, which are finally delivered to the load. The capacitors C_f are required for basic operation of the structure and filter the output voltage, thus eliminating the need for additional output filters.

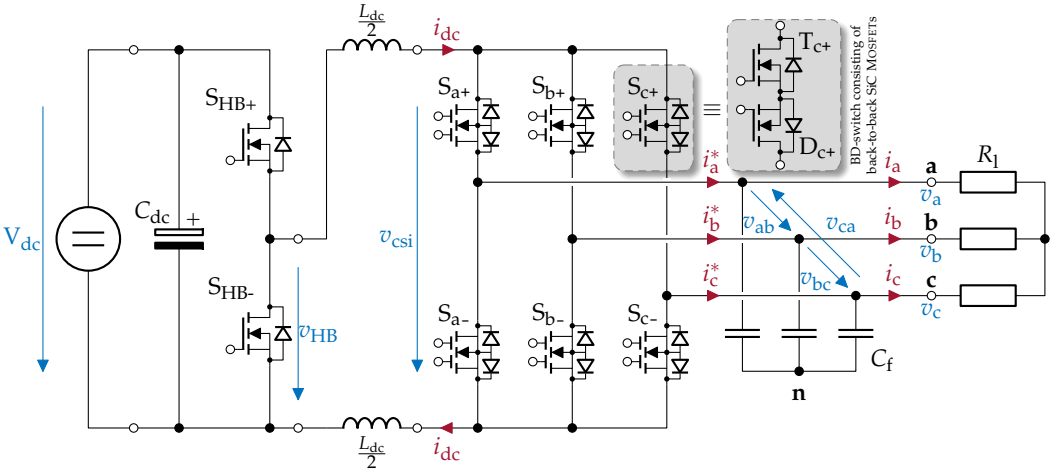

Figure 1. Basic circuit diagram of the CSI with a buck-stage input connected to a three-phase resistive load R_l. The reverse-blocking semiconductor switches are represented by MOSFETs arranged in a back-to-back (common source) configuration, and the DC-link inductor is split between the positive and negative rails.

A key advantage of the CSI is its inherent boost capability, allowing for a broader output voltage range compared to VSIs. Furthermore, the filter inductance of the single-phase buck-stage can be shared with the CSI, optimizing the system's overall design, as shown in Figure 1 [3].

Several publications are already available dealing with the practical design of compact and efficient current source inverter prototypes for low-voltage applications. The authors of [9,10] presented a 2.5 kW three-phase back-to-back CSI prototype based on normally-on SiC JFETs for motor drives. The researchers of [11,12] introduced the design of a compact 5 kW CSI based on back-to-back SiC MOSFETs for the non-isolated grid connection of photovoltaic panels. With their 48 V current source inverter prototype based on back-to-back GaN switches, the authors of [13] showed that CSIs also offer advantages for lower-power applications in axial flux PMSM drives with low inductance. The group that presented [14–16], on the other hand, has been using the CSI topology to build a 3 kW grid-connected three-phase integrated modular motor drive (PMSM). Here, too, back-to-back SiC MOSFETs are used for both the rectifiers and the inverter stage. Most recently, the authors of [17–19] presented a grid-connected ultra-compact high-efficiency 10 kW back-to-back SiC MOSFET current source rectifier for electric vehicle charging. In addition to the rectifier stage, the prototype also includes the necessary line filter stage to fulfill the requirements of CISPR 11 class A. All the works listed show high-performance converters for their application, but they lack a comprehensive description of an overall design process—e.g., the practical design of individual elements such as filter capacitors, the DC-link inductor, and power semiconductor switches and the losses that occur therein.

Other works deal in more detail with partial aspects of CSIs, with publications [20–27] focusing on layout parasitics and modeling of the power semiconductor losses for CSIs. Additionally, refernece [28] introduces a detailed switching loss model for the later used modulation scheme. The works in [29–32], on the other hand, present design methods for DC-link inductors that are specifically tailored to CSIs, while [32,33] deal more specifically with the design and modeling of filter capacitor-related quantities. More general theoretical

concepts for the design of CSIs are described in [2,34]; however, the aforementioned publications contain theoretical derivations as well.

In this paper, on the other hand, the design concepts of the individual aspects of the CSI are summarized, discussed in detail, and extended by analytical and numerical relationships. All required design steps including the sizing of passive components such as the filter capacitors and DC-link inductor are addressed. The proposed design incorporates a split DC-link inductor and filter capacitors in star (Y) connection to enhance the common-mode performance of the CSI.

A detailed loss analysis is conducted, focusing on the main contributors to system losses, namely, power semiconductor losses (conduction and switching losses) and DC-link inductor losses. Based on the design framework, a laboratory hardware prototype CSI with the specifications given in Table 1 is developed, built, and tested. The theoretical findings based on analytical models are then compared to the experimental results taken from the constructed hardware prototype.

As a modulation strategy, a symmetric pulse-width modulation (PWM) scheme with reduced common-mode voltage as described in [28,35,36] is used. For all computations and analyses, unity power factor is assumed. Please note that, although the converter prototype that is presented later contains a buck-stage at the input, only the inverter stage is considered in the presented design process.

Table 1. Prototype specifications.

Parameter	Symbol	Value
Nominal output power	P_{ac}	3 kW
Nominal output voltage	V_{ac}	200 V
Nominal output current	I_{ac}	5 A
DC-link current	$\bar{i}_{dc}$	7 A
Design switching frequency	f_{pwm}	100 kHz

2. Basic Operating Principle of CSI

The CSI structure requires power semiconductor switches with reverse voltage-blocking (RB) capability, while conducting current only in one direction, which prevents potentially destructive short- and open-circuit events during commutations. The RB capability can be implemented using different configurations. One approach is the combination of a reverse-conducting switch with a diode in series to implement the RB capability, as shown in Figure 2a for a Si or SiC MOSFET and Figure 2b for a GaN HEMT.

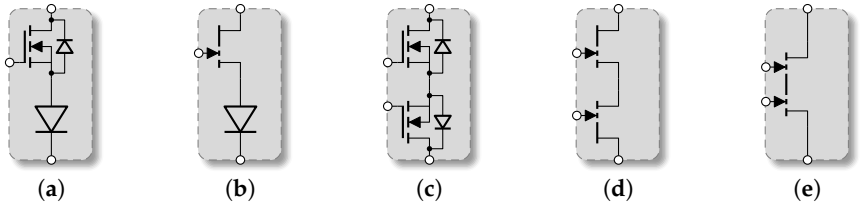

Figure 2. Different implementations of a reverse-blocking switch based on WBG power semiconductors: (**a**) SiC MOSFET with diode, (**b**) GaN HEMT with diode, (**c**) back-to-back connection of SiC MOSFETs in common source arrangement, (**d**) Dual GaN-HEMT, and (**e**) monolithic BD GaN-HEMT.

Another approach is the arrangement of two MOSFETs or GaN high-electron-mobility transistors (HEMT) in a back-to-back configuration, as illustrated in Figure 2c,d either in the common source or icommon drain configuration. All these approaches result in increased conduction losses compared to a single switch. Due to the limited voltage blocking capability of today's commercially available GaN devices, a back-to-back configuration of

SiC MOSFETs in common source arrangement is used in the presented prototype, which reduces conduction losses compared to the two diode-based approaches shown in Figure 2a,b.

The reverse blocking switches can also be implemented using IGBTs. Standard IGBTs do not show reverse-blocking capability and specially designed reverse-blocking IGBTs show an increased forward voltage drop and are not widespread. A combination of a conventional IGBT and a diode similar to Figure 2a,b would, of course, be possible; however, it would suffer from the forward voltage drop of two bipolar devices, and the limited switching frequency of a few tens of kHz of these devices would greatly increase the required DC-link inductance, compromising the power density of the prototype system.

The lateral structure of GaN HEMT, on the other hand, allows the implementation of dual-gate monolithic bidirectional switches (M-BDSs) with a shared drift region and two gates for blocking either voltage polarity [37–39]. However, for SiC-MOSFETs, a custom implementation as summarized in Figure 2 is required.

Like the VSI, space vector modulation (SVM) or carrier-based modulation (CBM) can be used to generate arbitrary three-phase inverter output currents. Both types of modulation provide similar results for the calculation of the output switching states, whereby SVM is mathematically more complex to execute but allows a more flexible implementation of different modulation schemes. In this work, SVM is used to describe the CSI operating principle, with [20,21] providing a comprehensive description of different optimized SVM techniques. An example of a CBM approach in CSIs can be found in [40].

Unlike the VSI topology with its three bridge-legs, the CSI structure comprises only two fundamental building blocks: the upper three-way switch, formed by S_{a+}, S_{b+}, and S_{c+}, and the lower three-way switch, consisting of S_{a-}, S_{b-}, and S_{c-} (see Figure 1). The permissible states for these switches ensure that, except during commutations, only one upper and one lower switch is turned on at any given time to conduct the DC-link current.

This constraint results in nine possible switching states, with six active states, meaning that they produce a non-zero current flow for i_a^*, i_b^*, or i_c^* (e.g., when S_{a+} and S_{b-} are turned on). The remaining three states are zero (or freewheeling) states, where the upper and lower switch of the same phase are turned on, resulting in circulating current in the inverter stage but zero current in i_a^*, i_b^*, and i_c^* (e.g., when S_{a+} and S_{a-} are turned on). The respective three-phase currents of each state can then be transformed into the complex current phasor $\underline{i}^*$ using the complex Clarke transformation, given as follows [41,42]:

$$\underline{i}^* = \frac{2}{3}\left[1 \; \mathrm{e}^{\mathrm{j}\frac{-2\pi}{3}} \; \mathrm{e}^{\mathrm{j}\frac{2\pi}{3}}\right] \cdot \begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix}. \tag{1}$$

The complex representations of the nine different states ($\underline{i}_1^*, \ldots, \underline{i}_9^*$) of the CSI are normalized by the average DC-link current $\bar{i}_{dc}$, yielding nine space vectors $\underline{I}_1, \ldots, \underline{I}_9$ (e.g., $\underline{I}_1 = \underline{i}_1^*/\bar{i}_{dc}$). A graphical representation of these discrete space vectors in a complex plane representation is shown in Figure 3.

The six space vectors of the active states divide the complex plane into six sectors, Ⅰ to Ⅵ, with each sector bounded by two space vectors denominated with $\underline{I}_x$ for the vector in the counter-clockwise direction and $\underline{I}_y$ in the clockwise direction (e.g., sector Ⅰ is bounded by $\underline{I}_x = \underline{I}_6$ and $\underline{I}_y = \underline{I}_1$). An arbitrary space vector $\underline{m} = M\,\mathrm{e}^{\mathrm{j}\,\varphi_m}$ can be synthesized as a linear combination of the surrounding vectors, i.e., the two vectors bounding the sector in which the desired space vector resides and one zero space vector. In this article, the term modulation index refers to M, the term angle of the modulation index denotes φ_m, and the term complex modulation index represents $\underline{m}$.

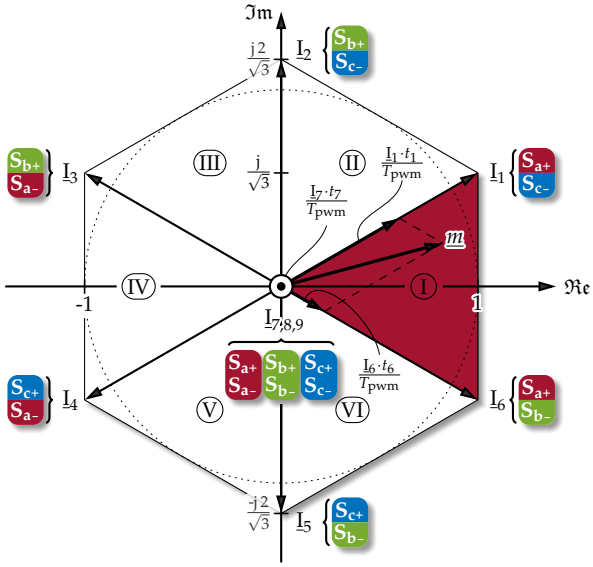

Figure 3. Space vector diagram for the CSI with six active space vectors ($\underline{I}_1, \ldots, \underline{I}_6$) and three zero space vectors ($\underline{I}_7, \underline{I}_8, \underline{I}_9$), dividing the complex plane into a hexagon with six sectors ($\textcircled{I}, \ldots, \textcircled{VI}$). The conducting switches of each phase are color coded (phase a: red; phase b: green; and phase c: blue).

In the PWM scheme, within one switching period T_{pwm}, the two states representing the bounding space vectors and one arbitrarily selectable zero space vector are applied for specific durations. These time intervals are denoted by t_x for $\underline{I}_x$, t_y for $\underline{I}_y$, and t_0 for the zero state, respectively, as illustrated in Figure 3. Please note that the sequence in which each vector is applied within a PWM period impacts switching losses, DC-link current ripple, output voltage ripple, and common-mode voltage, and therefore needs to be chosen wisely.

The resulting average switch node current can be analytically calculated by multiplying $\underline{m}$ by the DC-link current $\overline{\underline{i}^*} = \bar{i}_{\text{dc}} \cdot \underline{m}$. A locally averaged three-phase sinusoidal output current is generated by rotating $\underline{m}$ at a specific angular velocity. As the high-frequency AC component of $\underline{i}^*$ is filtered by the filter capacitors, the averaged switch node currents correspond to the inverter's output currents $\left(\text{avg}(\underline{i}^*) = \underline{i}\right.$ where $\underline{i}$ is the complex representation of the output currents i_{a}, i_{b}, and $\left.i_{\text{c}}\right)$ according to Equation (1).

3. Power Semiconductor Losses

This section provides an overview of the losses occurring in the power semiconductor devices used in the CSI. These losses can be separated into switching losses and conduction losses. Section 3.1 examines the switching loss mechanisms specific to the CSI and the proposed modulation scheme. It also presents measurement results obtained from a developed commutation cell prototype, which are then used to estimate the total switching losses of the inverter. The conduction losses of the CSI are addressed in Section 3.2, where a simple thermal model is also introduced to account for the heating effects on the power semiconductor switches.

3.1. Switching Losses

As previously discussed, the fundamental switching process in CSIs differs significantly from that in VSIs. In CSIs, the DC-link current commutates between two upper switches (e.g., from S_{a+} to S_{b+}), while a single lower switch remains active. Similarly, commutation occurs between two lower switches while an upper switch remains on. Unlike VSIs, where the basic switching cell is a half-bridge, CSIs use a three-way switch as the fundamental building block. This three-way switch consists of either all upper or all lower

switches, each enabling current flow in a specific direction. Figure 4 provides a simplified illustration of the current commutation process during a single switching event. In this process, the commutation current i_c represents the DC-link current, while the commutation voltage v_c corresponds to the line-to-line output voltage across the filter capacitors. The polarity of i_c and v_c determines whether the commutation results in a hard or soft switching event. As back-to-back connected MOSFETs are used to implement RB switches, a four-step commutation sequence is required to prevent a short-circuit of the commutation voltage [16]. In Figure 4a, a hard switching event is shown for the commutation between two upper switches when v_c has a positive polarity, and in Figure 4b, a soft-switching transition is given for positive i_c when the commutation voltage v_c is negative. For negative currents, the conditions for hard and soft switching are reversed, depending on the polarity of v_c.

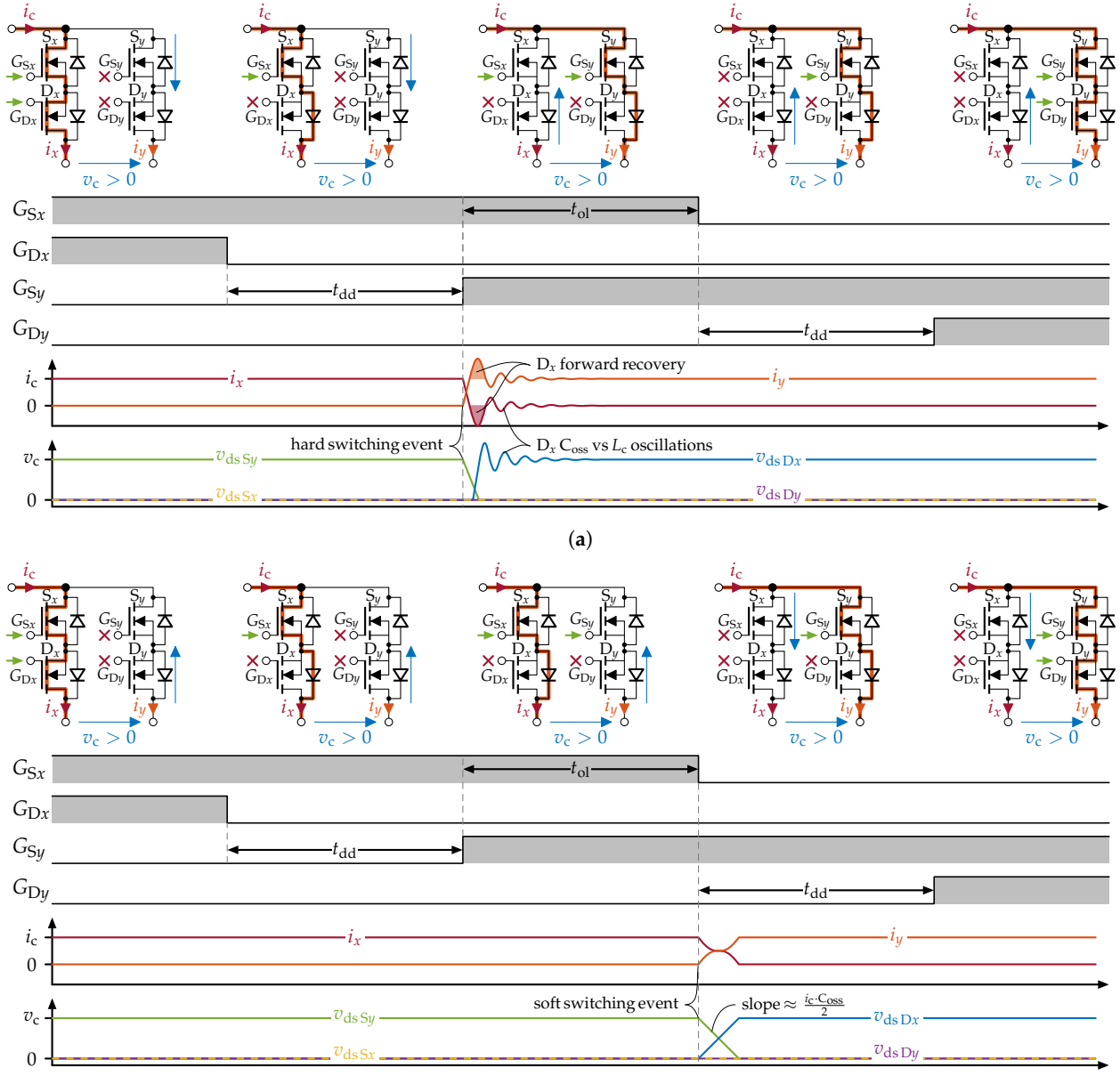

Figure 4. Schematic description of hard and soft commutation in the CSI during the four-step commutation for reverse-blocking switches in the back-to back configuration. (**a**) Hard switching commutation process for a positive commutation voltage v_c and positive commutation current i_c and (**b**) soft switching commutation for negative commutation voltage and positive commutation current.

In the initial state of both commutation processes, the two switches, S_x and D_x, are on, allowing i_c to flow through branch x. Depending on the polarity of v_c, either S_y (see Figure 4a) or D_y (see Figure 4b) blocks the voltage in this state. To prevent a short circuit of v_c, D_x is turned off in the first step, causing i_x to transition from the MOSFET channel to its body diode. After the diode delay time t_{dd} elapses, S_y is activated in the second step for the overlap duration t_{ol}, during which both active switches S_x and S_y are turned on simultaneously. In Figure 4a, where v_c is positive, i_c undergoes a hard commutation to branch y immediately. As the current in branch x decays, charge carriers in the D_x junction are cleared (forward recovery), momentarily resulting in negative current flow. Following this, D_x takes over the voltage v_c, with its output capacitance oscillating against the inductance of the commutation loop L_c. For simplicity, these parasitic elements are omitted from Figure 4. Finally, in the third step, S_x can be turned off losslessly.

In Figure 4b, with negative v_c, no immediate action occurs during the overlap period, since S_y can be turned on losslessly and i_c continues to flow through branch x. Once t_{ol} elapses and S_x is turned off, the current commutates to branch y. During this, the output capacitance of S_x charges with approximately $i_c/2$, while the output capacitance of D_y discharges by the same amount. The duration of this process depends on the output capacitance values and the DC-link current. In the fourth step, D_y is turned on in both cases, allowing i_y to transition from the body diode to the MOSFET channel, reducing on-state losses.

It is difficult to accurately model the switching losses of hard and soft switching commutations with data sheet values, and measurement of switching loss energies is essential to accurately model these switching losses.

A detailed description of the switching loss measurement and the resulting modeling of the switching losses can be found in [43]. However, as diodes are used in this publication to achieve the RVB capability of the switching elements and the loss modeling is carried out using a more simplified mathematical model, the switching loss measurement and the results are briefly described again in this paper.

As shown in [43], the simplified configuration displayed in Figure 5b can be used to measure the associated hard and soft switching losses without the need for a complete converter design. In this setup, only the two RB switching elements involved in the commutation process, denoted as S_x, D_x, S_y, and D_y, are implemented.

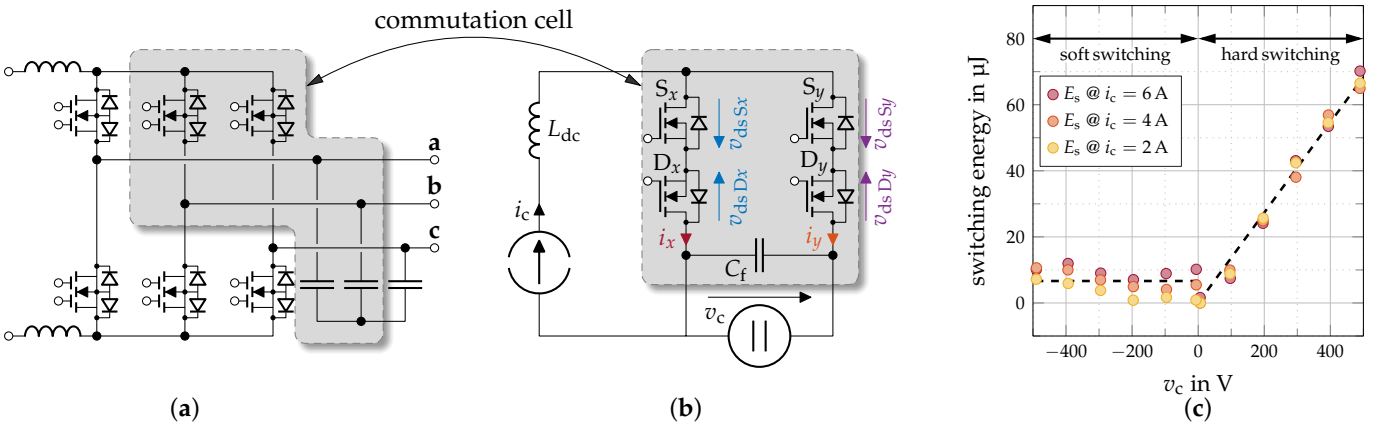

Figure 5. Switching loss measurement for CSIs. (**a**) Basic circuit diagram of the CSI. (**b**) Commutation cell derived from the CSI used to measure switching losses and (**c**) measured switching energies of SiC MOSFETs IMBG65R072M1H as a function of commutation voltage at commutation currents i_c = 2 A, 4 A, and 6 A. A simple switching loss model given in Equation (2) is derived from the measurement results.

The commutation current i_c, i.e., the DC-link current, is injected into the commutation inductor L_{dc}, which emulates the DC-link of a full converter. Meanwhile, the commutation voltage v_c, representing the line-to-line output voltage, is controlled via an external voltage source connected to the commutation cell filter capacitance C_f. This configuration allows for independent control of i_c and v_c, enabling precise characterization of switching losses as a function of these parameters. Unlike the half-bridge circuits commonly used in VSIs or other CSI switching-loss measurements discussed in the literature [24,25,44], this experimental setup requires only a single-pulse test rather than a double-pulse test as the commutation voltage can be directly adjusted by the external voltage source C_{com}. These measurements are crucial, as the switching losses are highly dependent on the commutation loop inductance, which is influenced by the board layout and the physical placement of the switches and filter capacitors.

Therefore, the commutation cell has been designed to closely replicate the layout of the full converter. To achieve this, the filter capacitors were positioned as near as possible to the power semiconductor switches, minimizing the commutation loop inductance and thereby reducing switching losses. The power semiconductor switches used in the measurement (IMBG65R072M1H) were operated with a gate voltage of 18 V during turn-on and -2 V during turn-off. In Figure 5c, the total measured switching loss energies across all four involved SiC MOSFETs IMBG65R072M1H conducted on this commutation cell are given as a function of commutation voltage v_c.

According to Figure 5c, neither the hard nor the soft switching losses vary significantly with changes in the commutation current i_c. In the soft switching region, characterized by negative commutation voltages, the switching energy remains nearly constant and is largely unaffected by the commutation voltage. However, in the hard switching region with positive commutation voltages, the switching losses increase linearly with the commutation voltage. This leads to the development of the simplified analytic switching loss model

$$E_s(v_c, i_c) = \begin{cases} E_{soft} = k_{soft} & \forall \begin{smallmatrix} v_c<0 \,\&\, i_c\geq 0 \\ v_c\geq 0 \,\&\, i_c<0 \end{smallmatrix} \\ E_{hard} = k_{hard}\, v_c & \forall \begin{smallmatrix} v_c\geq 0 \,\&\, i_c\geq 0 \\ v_c< \,\&\, i_c<0 \end{smallmatrix} \end{cases} \tag{2}$$

modeling the dashed lines in Figure 5c.

Based on the presented switching loss measurements, the two parameters for hard and soft switching can be determined as $k_{hard} = 137\,\text{nJ V}^{-1}$ and $k_{soft} = 6.64\,\mu\text{J}$ for the switching cell at hand. It is important to note that this switching loss model focuses exclusively on the two switching elements involved in a single commutation event and does not account for losses caused by the voltage change in the third switch, as discussed in [38]. In this simplified switching loss model, unified switching loss energies are used for all three branches, not considering the fact that commutation between the phases with increased commutation loop inductance may lead to higher switching loss energies.

The total switching losses depend on several factors such as the chosen modulation scheme, the number of switching transitions (which is influenced by the PWM frequency), and the associated commutation voltages and currents for each transition. The switching losses are furthermore affected by the applied commutation sequence. The objective of the modulation scheme is to minimize switching losses, to reduce DC-link current ripple, and to allow for the smallest possible DC-link inductor design, while also keeping the common-mode output voltage as low as possible. Previous studies have compared various modulation schemes with respect to these parameters [20,21,28,35,36,45] and found that the Reduced Voltage Modulation (RVM) strategy (naming scheme according to [28]) yields the lowest switching losses and DC-link current ripple, while also providing the lowest common-mode output voltage. Furthermore, RVM is a symmetric PWM scheme,

which simplifies the measurement of DC-link current and output quantities (voltages and currents), as sampling in the middle of the PWM period automatically yields their average values.

Table 2 summarizes the turn-on and turn-off sequences of the inverter's power semiconductor switches during one PWM period for each sector, based on the polarities of the line-to-line output voltages. The voltages indicated above and below the arrows represent the respective commutation voltage v_c as defined in Equation (2).

Table 2. Switching cycles of the RB semiconductor switches during one PWM period for the RVM strategy in sectors Ⅰ, Ⅱ, and Ⅲ (cf. Figure 3). Soft switching transitions are indicated by a filled arrow, while hard switching transitions are indicated by an unfilled arrow.

Sector	Condition	Switching Cycle (• $v_c > 0$, • $v_c < 0$)
Ⅰ	$v_{bc} < 0$	$S_{c+}S_{c-} \xrightarrow{v_{ca}} S_{a+}S_{c-} \xrightarrow{-v_{bc}} S_{a+}S_{b-} \Rightarrow S_{a+}S_{c-} \xrightarrow{-v_{ca}} S_{c+}S_{c-}$
	$v_{bc} > 0$	$S_{b+}S_{b-} \xrightarrow{-v_{ab}} S_{a+}S_{b-} \xrightarrow{v_{bc}} S_{a+}S_{c-} \Rightarrow S_{a+}S_{b-} \xrightarrow{v_{ab}} S_{b+}S_{b-}$
Ⅱ	$v_{ab} > 0$	$S_{b+}S_{b-} \xrightarrow{v_{bc}} S_{b+}S_{c-} \xrightarrow{-v_{ab}} S_{a+}S_{c-} \Rightarrow S_{b+}S_{c-} \xrightarrow{-v_{bc}} S_{b+}S_{b-}$
	$v_{ab} < 0$	$S_{a+}S_{a-} \xrightarrow{-v_{ca}} S_{a+}S_{c-} \xrightarrow{v_{ab}} S_{b+}S_{c-} \Rightarrow S_{a+}S_{c-} \xrightarrow{v_{ca}} S_{a+}S_{a-}$
Ⅲ	$v_{ca} < 0$	$S_{a+}S_{a-} \xrightarrow{v_{ab}} S_{b+}S_{a-} \xrightarrow{-v_{ca}} S_{b+}S_{c-} \Rightarrow S_{b+}S_{a-} \xrightarrow{-v_{ab}} S_{a+}S_{a-}$
	$v_{ca} > 0$	$S_{c+}S_{c-} \xrightarrow{-v_{bc}} S_{b+}S_{c-} \xrightarrow{v_{ca}} S_{b+}S_{a-} \Rightarrow S_{b+}S_{c-} \xrightarrow{v_{bc}} S_{c+}S_{c-}$

If the voltage symbol appears above an arrow, the commutation occurs between two upper switches with a positive commutation current. Conversely, if the voltage symbol is below the arrow, the commutation occurs between two lower switches with a negative commutation current. A positive commutation voltage is indicated by a red color, while a negative commutation voltage is shown in blue. Furthermore, the distinction between hard and soft switching transitions is indicated by filled and unfilled arrows, respectively. Filled arrows represent soft switching events and unfilled arrows represent hard switching events.

Figure 6 illustrates the expected line-to-line output voltage waveforms at unity power factor, with an emphasis on the corresponding voltages for hard and soft switching in sector Ⅱ. At unity power factor, the voltage condition ($v_{ab} > 0$ or $v_{ab} < 0$) for selecting the switching sequence changes at the midpoint of the sector. As a result, the line-to-line voltage with the highest amplitude is never involved in a commutation event in the RVM strategy.

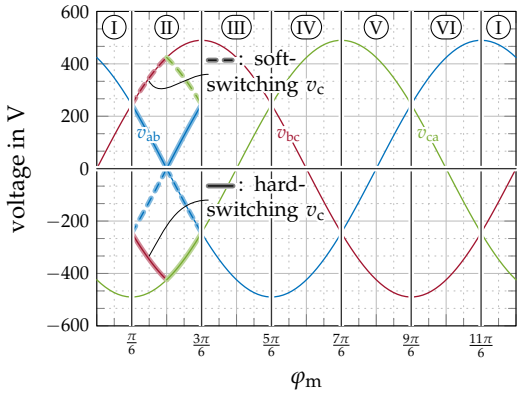

Figure 6. Ideal line-to-line voltage waveforms at unity power factor. For sector Ⅱ, the switching voltages for the respective commutation sequence are displayed according to Table 2. Solid bold lines indicate hard switching events in sector Ⅱ whereas dashed lines indicate soft switching events.

According to the switching scheme presented in Table 2, the commutation current in sector Ⅱ, where $v_{ab} > 0$ (with $\varphi_m = \frac{\pi}{6} \dots \frac{2\pi}{6}$ for unity power factor), remains positive throughout the sector as switching operations only occur between the three upper switches S_{a+}, S_{b+}, and S_{c+}. This results in two hard switching transitions involving v_{ab} and $-v_{bc}$, and two soft switching commutations involving $-v_{ab}$ and v_{bc}. The switching losses for this commutation sequence averaged over half sector Ⅱ ($\frac{\pi}{6} \dots \frac{2\pi}{6}$) can therefore be calculated by

$$\begin{aligned} P_s &= \frac{f_{pwm}}{\frac{\pi}{6}} \cdot \int_{\frac{\pi}{6}}^{\frac{2\pi}{6}} E_{soft}(v_{bc}) + E_{soft}(-v_{ab}) + E_{hard}(v_{ab}) + E_{hard}(-v_{bc})\, d\varphi \\ &= \frac{3\sqrt{3}\, f_{pwm}}{\pi} \cdot \left(k_{soft} + k_{hard} \cdot \sqrt{2}\, V_{ac}\right) \end{aligned} \tag{3}$$

where f_{pwm} denotes the PWM switching frequency and k_{hard} and k_{soft} represent the constants for hard and soft switching, respectively, as defined in the proposed switching loss model in Equation (2). The current $\bar{i}_{dc}$ is the maximum average DC-link current, and V_{ac} is the maximum RMS value of the output phase voltage. For a switching frequency of $f_{pwm} = 100\,\text{kHz}$ and a maximum RMS output voltage of $V_{ac} = 200\,\text{V}$, the switching losses can be estimated to $P_s = 7.51\,\text{W}$. If the output voltage is assumed to change linearly with the modulation index, e.g., for resistive loads, the switching losses over the entire output load range can also be estimated. A graphical representation of these losses is shown in Figure 7, where the switching losses are stacked on top of the later calculated conduction losses.

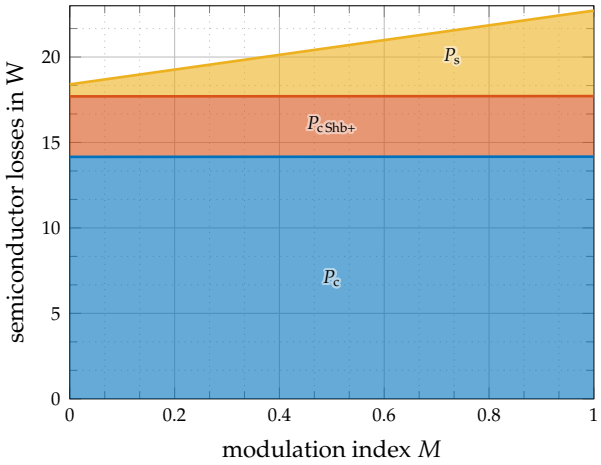

Figure 7. Power semiconductor switching and conduction losses at different modulation indices M for a linear load model.

3.2. Conduction Losses

Conduction losses in the CSI are straightforward to calculate, as the DC-link current flows through four devices at any given time: one upper switch, one upper reverse-blocking element, one lower switch, and one lower reverse-blocking element. The average conduction losses per fundamental period T at the output can be estimated by

$$P_c = 4 \cdot R_{ds(on)} \cdot \frac{1}{T} \cdot \int_0^T i_{dc}^2\, dt \tag{4}$$

using the device on-resistance $R_{ds(on)}$, as provided in the datasheet. For a constant DC-link current, this simplifies to

$$P_c = 4 \cdot R_{ds(on)} \cdot \bar{i}_{dc}^2. \tag{5}$$

The used semiconductor switches are operated with a gate voltage of 18 V during turn-on and the corresponding on-state resistance at a junction temperature of $T_j = 25\,^\circ\mathrm{C}$ is 72 mΩ. For a junction temperature of $T_j = 150\,^\circ\mathrm{C}$, the resistance increases to 101 mΩ. At $T_j = 25\,^\circ\mathrm{C}$, the conduction losses are calculated as $P_c = 14.1\,\mathrm{W}$. In the later-developed prototype, the upper switch of the included buck stage is continuously turned-on and experiences conduction losses. These losses must be modeled as well. The conduction losses in the buck stage can be calculated using the same approach as for the main inverter. Specifically, the conduction losses in the upper switch of the buck stage are given by $P_{c\,\mathrm{Shb+}} = R_{\mathrm{ds(on)}} \cdot \bar{i}_{\mathrm{dc}}^2 = 3.53\,\mathrm{W}$.

Considering the thermal management system (heat-sink and fans), the temperature rise—and consequently, the increase in $R_{\mathrm{ds(on)}}$ and conduction losses can be estimated iteratively. The first step is to gather the thermal resistance data for each thermal interface. SMD-mounted, bottom-side-cooled MOSFET devices are used—i.e., the thermal resistances of the thermal vias as well as the thermal resistances of the interface material from the PCB to the heat sink have to be considered next to the thermal resistance of the MOSFET itself. According to the technical datasheet, each of the 13 semiconductor switches (12 switches in the inverter and the half-bridge top switch) has a thermal junction-to-case resistance of $R_{\mathrm{th,JC}} = 1.07\,\mathrm{K\,W^{-1}}$. Not only the thermal resistance of the MOSFETs has to be considered but also the thermal vias beneath the SMD-mounted devices. The thermal resistance of the vias beneath the TO-263-7 packages is estimated to $R_{\mathrm{th,via}} = 0.08\,\mathrm{K\,W^{-1}}$, and the thermal resistance of the interface pad between the heat sink and PCB is $R_{\mathrm{th,pad}} = 0.7\,\mathrm{K\,W^{-1}}$. The thermal resistance of the pure-copper heat sink to ambient air, based on its geometry and fan airflow rate of $9.4\,\mathrm{m^3\,h^{-1}}$, is $R_{\mathrm{th,hs}} = 0.27\,\mathrm{K\,W^{-1}}$. A graphical representation of the thermal stackup including all thermal resistances is shown in Figure 8.

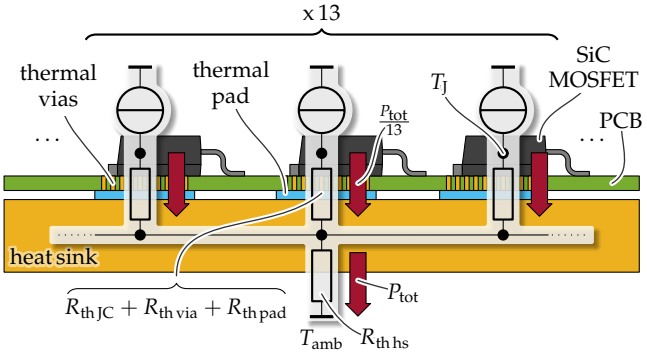

Figure 8. Illustration of the power semiconductor switches and the associated thermal management system. The switches in the TO-263-7 housing are soldered directly to the circuit board. Thermal vias then dissipate the power loss via a heat conducting pad to the heat sink, which is cooled by an active air flow.

For simplicity, we assume that all semiconductor switches experience the same losses, regardless of whether the device is acting as an active switch or as a reverse-blocking device. The total thermal resistance $R_{\mathrm{th,tot}}$ from junction to ambient can then be estimated by

$$R_{\mathrm{th\,tot}} = \frac{R_{\mathrm{th\,JC}} + R_{\mathrm{th\,via}} + R_{\mathrm{th\,pad}}}{13} + R_{\mathrm{th\,hs}} = 0.412\,\mathrm{K\,W^{-1}}. \tag{6}$$

With this thermal resistance, the actual junction temperature can be calculated, which finally impacts conduction losses due to the thermal dependency of the $R_{\mathrm{ds(on)}}$. The temperature rise is calculated iteratively using

$$T_J^{\langle n \rangle} = T_{\mathrm{amb}} + \left(P_s + P_c\left(T_J^{\langle n-1 \rangle}\right) + P_{c\,\mathrm{Shb+}}\left(T_J^{\langle n-1 \rangle}\right)\right) \cdot R_{\mathrm{th\,tot}}. \tag{7}$$

In this equation, the iteration starts with an initial junction and ambient temperature of $T_{\mathrm{J}}^{\langle 0 \rangle} = T_{\mathrm{amb}} = 25\,^{\circ}\mathrm{C}$. The relationship between $R_{\mathrm{ds(on)}}$ and junction temperature T_{J} is taken from the manufacturer's datasheet. After 10 iterations, the change in the resulting increase in temperature converges, and the maximum conduction losses are calculated as $P_{\mathrm{c}} = 14.18\,\mathrm{W}$ and $P_{\mathrm{c,Shb+}} = 3.54\,\mathrm{W}$ at a junction temperature of $T_{\mathrm{J}} = 35.4\,^{\circ}\mathrm{C}$. This estimation represents the worst-case scenario at a modulation index of $M = 1$ and a maximum RMS output voltage of $V_{\mathrm{ac}} = 200\,\mathrm{V}$, where switching losses are the highest.

By assuming a linear resistive load where the output voltage decreases proportionally with the modulation index, the same iterative procedure can be applied across multiple operating points. The resulting power semiconductor losses, including the conduction losses from the previous section for the inverter structure, are displayed in Figure 7.

It can be observed that both the conduction losses of the inverter stage and the upper switch of the half-bridge remain constant across the entire range of modulation indices, despite an increase in switching losses towards higher modulation indices due to elevated switching losses. Conversely, the switching losses, as anticipated, exhibit a nearly linear increase with increasing modulation index. However, total semiconductor losses are predominantly influenced by conduction losses.

4. Design of the Passive Components

This section outlines the design process of the passive components of the CSI, namely, the DC-link inductor and filter capacitors, using the space vector modulation strategy discussed in Section 2. The key design parameters for the filter capacitors are the capacitance value C_{f}, the peak-to-peak voltage ripple Δv_{max}, the maximum RMS current $I_{\mathrm{C\,max}}$, and the maximum voltage v_{max} across the capacitors. The design parameters for the DC-link inductor include the inductance value L_{dc}, the peak-to-peak current ripple $\Delta i_{\mathrm{dc\,max}}$, the maximum RMS current $I_{\mathrm{dc\,max}}$, and the peak current $\bar{i}_{\mathrm{dc\,max}}$.

The design process for both capacitors and inductors begins with determining the required time intervals for each space vector in the modulation process. Therefore, the sector that contains the desired space vector $\underline{m}$ must be identified. As already shown in Section 2, $\underline{m}$ is synthesized as a linear combination of the two adjacent active space vectors $\underline{\mathrm{I}}_x$ and $\underline{\mathrm{I}}_y$, along with a selected zero vector, as specified in Table 2. The time intervals t_x and t_y for the active vectors are calculated by solving

$$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = T_{\mathrm{pwm}} \cdot \begin{bmatrix} \Re\mathfrak{e}(\underline{\mathrm{I}}_x) & \Im\mathfrak{m}(\underline{\mathrm{I}}_x) \\ \Re\mathfrak{e}(\underline{\mathrm{I}}_y) & \Im\mathfrak{m}(\underline{\mathrm{I}}_y) \end{bmatrix}^{-1} \cdot \begin{bmatrix} \Re\mathfrak{e}(\underline{m}) \\ \Im\mathfrak{m}(\underline{m}) \end{bmatrix}. \tag{8}$$

The time interval for the zero space vector t_0 can be easily computed via the relationship $T_{\mathrm{pwm}} = t_x + t_y + t_0$. In sector (I), the three time intervals

$$\begin{bmatrix} t_{x\mathrm{I}} \\ t_{y\mathrm{I}} \\ t_{0\mathrm{I}} \end{bmatrix} = T_{\mathrm{pwm}} \cdot \begin{bmatrix} m\,\cos\left(\varphi_{\mathrm{m}} + \frac{\pi}{3}\right) \\ m\,\cos\left(\varphi_{\mathrm{m}} + \frac{5\pi}{3}\right) \\ 1 + m\,\cos(\varphi_{\mathrm{m}} + \pi) \end{bmatrix} \tag{9}$$

can be obtained using Equation (8). Due to the symmetric nature of the presented PWM scheme, the sequence within one PWM period begins with the application of the zero vector $\underline{\mathrm{I}}_0$ for the time interval $\frac{t_0}{2}$. This is followed by $\underline{\mathrm{I}}_x$ or $\underline{\mathrm{I}}_y$ for $\frac{t_x}{2}$ or $\frac{t_y}{2}$, depending on the applied sequence detailed in Table 2 for each sector and a certain line-to-line. The remaining space vector (t_x or t_y) is then applied for its full duration, after which the process reverses with $\underline{\mathrm{I}}_x$ or $\underline{\mathrm{I}}_y$ and ends with $\underline{\mathrm{I}}_0$.

4.1. Design of the Filter Capacitors

During a PWM period, the output currents i_a, i_b, and i_c, represented by the complex vector $\underline{i}$, are assumed to be constant. The complex switch node current $\underline{i}^*$ is determined by the applied space vector $\underline{m}$, which represents the switch state, and the constant DC-link current $\bar{i}_{dc}$. Consequently, the complex current vector flowing into the filter capacitors, $\underline{i}_C$, can be derived using Kirchhoff's Current Law (KCL) for each time interval. For instance, in Sector Ⅰ during the interval t_x, the capacitor current is expressed as

$$\underline{i}_C = \underline{i}_S - \underline{i} = \bar{i}_{dc} \cdot \underline{I}_6 - \bar{i}_{dc}\, M\, e^{j\varphi_m}. \tag{10}$$

This current remains constant over each separate time interval. During active states, the capacitors are charged by i_{dc}, while during zero states, the load current is supplied by the capacitors. The voltage change across the capacitors for each full time interval t_x, t_y, or t_0 can be calculated using the linearized capacitor equation

$$\begin{bmatrix} \Delta\underline{v}_x \\ \Delta\underline{v}_y \\ \Delta\underline{v}_0 \end{bmatrix} = \frac{\bar{i}_{dc}}{C_f} \cdot \begin{bmatrix} (\underline{I}_x - \underline{m}) \cdot t_x \\ (\underline{I}_y - \underline{m}) \cdot t_y \\ -\underline{m} \cdot t_0 \end{bmatrix}. \tag{11}$$

This expression can be evaluated for each sector and transformed back into phase quantities to calculate the phase voltage changes. For Sector Ⅰ, the voltage change in phase a during each full PWM interval is therefore given by

$$\begin{bmatrix} \Delta v_{x\mathrm{I}\,a} \\ \Delta v_{y\mathrm{I}\,a} \\ \Delta v_{0\mathrm{I}\,a} \end{bmatrix} = \frac{\bar{i}_{dc}\, T_{pwm}\, M}{C_f} \cdot \left(1 - m\, \cos(\varphi_m)\right) \cdot \begin{bmatrix} \cos\left(\varphi_m + \frac{\pi}{3}\right) \\ \cos\left(\varphi_m - \frac{\pi}{3}\right) \\ -\cos(\varphi_m) \end{bmatrix}. \tag{12}$$

In Figure 9, the voltage change per time interval in phase a across all sectors is shown for three different modulation indices, $M = 1$, $M = 2/3$, and $M = 1/3$. Please note that the waveforms presented illustrate the theoretical voltage changes over complete time intervals when the individual vectors are applied in a sequence. For the modulation scheme outlined in Table 2, certain time intervals are split, such as in sector Ⅰ when $v_{bc} > 0$, where the interval t_x is halved and the voltage ripple will be smaller than the voltage ripple curves given in Figure 9. To determine the overall voltage ripple envelope, a detailed analysis of the vector sequence is therefore required. The ripple components in phases b and c have the same basic shape but are shifted by $\frac{4\pi}{3}$ and $\frac{2\pi}{3}$, respectively. To compute the peak-to-peak output voltage ripple Δv_a in phase a, the modulation scheme and resulting waveforms must be analyzed.

In sectors Ⅰ and Ⅳ, $\Delta v_{0\,a}$ dominates the voltage ripple, as interval t_0 is never split in the applied symmetric PWM scheme, resulting in identical maximum ripple values for these sectors. In the other sectors, the calculation is more complex as $\Delta v_{x\,a}$ or $\Delta v_{y\,a}$ dominate the voltage ripple. For sector Ⅱ $v_{ab} < 0$, the x-interval splits into two parts, resulting in the application of the sequence $|\,\underline{I}_0 \rightarrow \underline{I}_x \rightarrow \underline{I}_y \rightarrow \underline{I}_x \rightarrow \underline{I}_0\,|$ according to Table 2. Here, $\underline{I}_0$ is applied twice for $t_0/2$, resulting in a total application time interval of t_0, taking into account the previous and subsequent PWM intervals. The intervals' center space vector $\underline{I}_y$ is also applied for its full duration t_y, but $\underline{I}_x$ is applied twice for $t_x/2$, resulting in only half the voltage change $\Delta v_{x\,a}/2$. This requires the maximum ripple to be determined as $\Delta v_a = \max\left(|\Delta v_{x\,a}/2|, |\Delta v_{y\,a}|, |\Delta v_{0\,a}|\right)$.

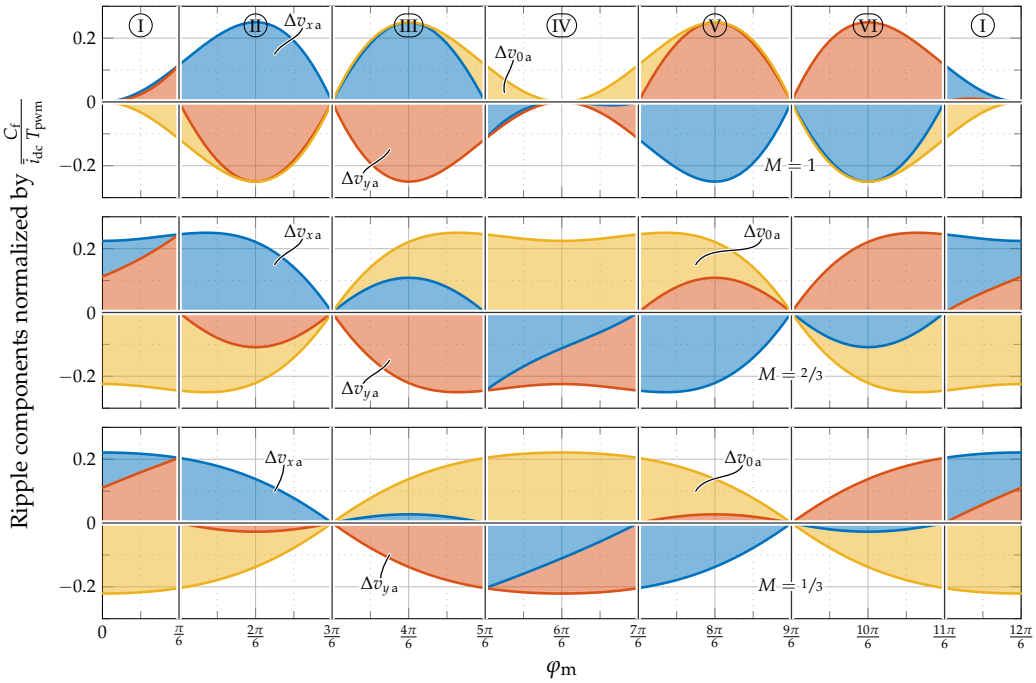

Figure 9. Normalized theoretical CSI voltage ripple components $\Delta v_{x\,a}$, $\Delta v_{y\,a}$, and $\Delta v_{0\,a}$ of phase a if the individual space vectors are applied for their full time intervals in a sequence and not according to the modulation scheme. The three stacked plots represent the components at modulation index $M = 1$, $M = 2/3$, and $M = 1/3$.

The different cases as well as the cases for the other relevant sectors are summarized in Equation (13), with the filled hexagon areas indicating the applicable equations for unity load power factor. Please note that these areas rotate accordingly for different power factors.

$$\Delta v_a(\underline{m}) = \frac{\bar{i}_{dc}\, T_{pwm}}{C_f} \cdot \begin{cases} M\,|\cos(\varphi_m)| - \quad M^2\cos^2(\varphi_m) & \forall\ \underline{m} \in \text{  } \\ M\,|\cos(\varphi_m)| - \frac{1}{2}M^2\cos^2(\varphi_m) - \frac{\sqrt{3}}{4}\,|\sin(2\,\varphi_m)| & \forall\ \underline{m} \in \text{  } \\ -\frac{1}{2}M^2\cos^2(\varphi_m) + \frac{\sqrt{3}}{4}\,|\sin(2\,\varphi_m)| & \forall\ \underline{m} \in \text{  } \end{cases} \tag{13}$$

The mathematical expressions defining the different regions, independent of the load power factor, are provided by

$$\begin{aligned} \text{  } &= \quad (v_{ab} \le 0\ \&\ v_{ca} \ge 0)\ |\ (v_{ab} \ge 0\ \&\ v_{ca} \le 0) \\ \text{  } &= \Big((v_{ab} \le 0\ \&\ v_{ca} \le 0)\ |\ (v_{ab} \ge 0\ \&\ v_{ca} \ge 0)\Big)\ \&\ \Big(M\,|\cos(\varphi_m)| \ge \tfrac{1}{\sqrt{3}}\Big) \\ \text{  } &= \Big((v_{ab} \le 0\ \&\ v_{ca} \le 0)\ |\ (v_{ab} \ge 0\ \&\ v_{ca} \ge 0)\Big)\ \&\ \Big(M\,|\cos(\varphi_m)| \le \tfrac{1}{\sqrt{3}}\Big) \end{aligned} \tag{14}$$

A graphical representation of the normalized ripple for different modulation indices is given in Figure 10 for the applied modulation strategy also highlighted in Table 2. Note that the steps in the curves at $\varphi_m = 2\pi/6$, $4\pi/6$, $8\pi/6$, and $10\pi/6$ are caused by the transitions of the modulation scheme according to Equation (14).

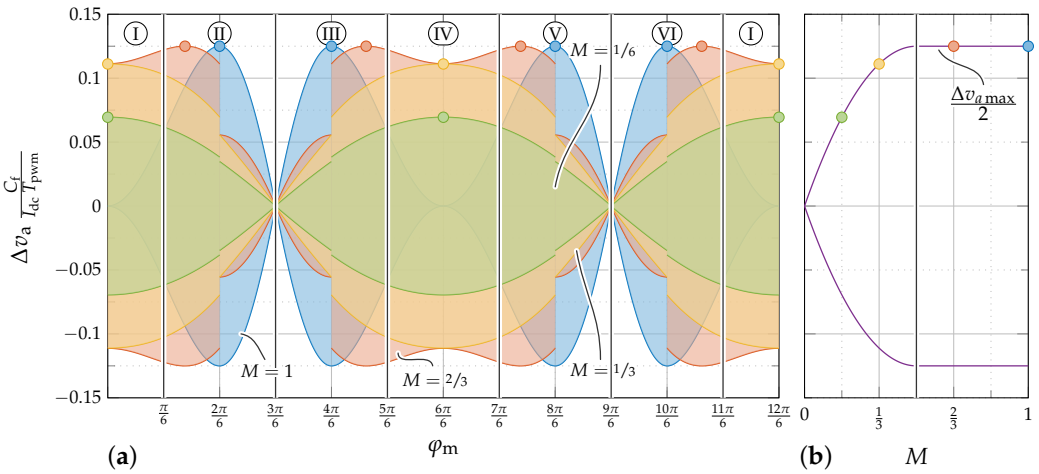

Figure 10. (**a**) ormalized output voltage ripple curves of the CSI applying the RVM strategy for different modulation indices M for a load power factor of one. The steps observable at $\frac{2\pi}{6}$, $\frac{4\pi}{6}$, $\frac{8\pi}{6}$, and $\frac{10\pi}{6}$ are caused by the transitions of the modulation scheme according to Equation (14). (**b**) Peak value of the capacitor voltage ripple as a function of the modulation index M.

The maximum output voltage ripple $\Delta v_{\max} = \bar{i}_{dc}\, T_{pwm}/4\, C_f$ can now be used to select the filter capacitor size. The allowable output voltage ripple $\Delta v_{\max}$ is evaluated using Equation (13) and finally leads to

$$C_f = \frac{\bar{i}_{dc}\, T_{pwm}}{4\, \Delta v_{\max}}. \tag{15}$$

It should be noted that $\Delta v_{\max}$ for $M \geq 1/2$ is independent of the load's power factor. Furthermore, the maximum voltage $v_{\max}$ across the capacitors can be estimated using the presented derivations. This maximum occurs when the peak voltage ripple coincides with the peak of the fundamental wave due to a non-unity load power factor and can be calculated using

$$v_{\max} = \sqrt{2}\, V_{ac} + \frac{\Delta v_{\max}}{2}. \tag{16}$$

The instantaneous RMS current through the capacitor in phase a can be computed for any reference space vector $\underline{m}$ based on the previous derivations and also using Equation (17).

$$I^*(\underline{m}) = \bar{i}_{dc} \cdot \sqrt{\frac{1}{T_{pwm}} \cdot \left[\Re\mathfrak{e}(\underline{I}_x)^2 \cdot t_x + \Re\mathfrak{e}(\underline{I}_y)^2 \cdot t_y\right]}. \tag{17}$$

The instantaneous RMS value of the output current in phase a can be similarly calculated via the mean value of the output current

$$I(\underline{m}) = \frac{\bar{i}_{dc}}{T_{pwm}} \cdot \left[\Re\mathfrak{e}(\underline{I}_x)\, t_x + \Re\mathfrak{e}(\underline{I}_y)\, t_y\right]. \tag{18}$$

Consequently, due to the orthogonality of the two signals, the RMS current flowing into the capacitor of phase a

$$I_C(\underline{m}) = \sqrt{(I^*)^2 - (I)^2} \tag{19}$$

is the geometric difference of the two. For sinusoidal signals, i.e., a rotating space vector, the global RMS values of the currents can be computed as well resulting in the switch node current

$$I^*(M) = \sqrt{\frac{3\,\bar{i}_{\mathrm{dc}}}{2\,\pi} \cdot \int_0^{2\pi} \Re\mathfrak{e}(\underline{\mathrm{I}}_x)^2 \cdot t_x + \Re\mathfrak{e}(\underline{\mathrm{I}}_y)^2 \cdot t_y \,\mathrm{d}\varphi_{\mathrm{m}}} = \bar{i}_{\mathrm{dc}} \cdot \sqrt{\tfrac{2\,M}{\pi}}. \tag{20}$$

The RMS value of the output currents can be computed by

$$I(M) = \sqrt{\left(M \cdot \frac{\bar{i}_{\mathrm{dc}}}{\sqrt{2}}\right)^2 - (\mathrm{C_f} \cdot 2\,\pi\, f \cdot V_{\mathrm{ac}})^2} \tag{21}$$

where the second part of the geometric difference describes the fundamental frequency current flow through the capacitor at f lowering the maximum achievable output current amplitude at higher frequencies. Consequently, the RMS capacitor current

$$I_{\mathrm{C}}(M) = \sqrt{\bar{i}_{\mathrm{dc}}^2 \cdot \left(\frac{2\,M}{\pi} - \frac{M^2}{2}\right) + (\mathrm{C_f} \cdot 2\,\pi\, f \cdot V_{\mathrm{ac}})^2}. \tag{22}$$

is again the geometric difference between the two. Independent of the second term, the maximum RMS capacitor current appears at $M = \frac{2}{\pi}$ and can be calculated by

$$I_{\mathrm{C\,max}} = \sqrt{\left(\bar{i}_{\mathrm{dc}} \cdot \frac{\sqrt{2}}{\pi}\right)^2 + (\mathrm{C_f} \cdot 2\,\pi\, f \cdot V_{\mathrm{ac}})^2}. \tag{23}$$

Note that the second term in Equation (23) considering the fundamental component of the capacitor current is typically smaller than the first term if the converter is properly designed. Furthermore, V_{ac} varies with M and Equation (23) represents a worst-case scenario for the RMS current. The maximum capacitor current $I_{\mathrm{C\,max}}$ can be calculated as 3.3 A for the converter at hand with $f_{\mathrm{max}} = 1$ kHz and $C_{\mathrm{f}} = 800\,\mu$F).

Based on Equations (15), (16) and (23), a suitable capacitor array is selected. Due to the challenging AC current requirement of these capacitors, film-type capacitors or C0G/NP0-based ceramic capacitors are required. If the output voltage ripple is limited to <10% of the maximum AC voltage, i.e., $\Delta v_{\mathrm{max}} < 28.3$ V for $\hat{V}_{\mathrm{ac}} = \sqrt{2}, V_{\mathrm{ac}}$, the minimum filter capacitance can be calculated to $C_{\mathrm{f}} = 619$ nF. To further reduce the output voltage ripple, however, a capacitor with $C_{\mathrm{f}} = 800$ nF has been selected.

The output capacitance finally implemented in the prototype using a parallel arrangement of 8 × 100 nF C0G MLCC capacitors (C5750NP02W104J280KA) in 2220 packages rated for 450 V. The maximum RMS current is 3.31 A at 100 kHz, which is well below the 8.675 A current rating per capacitor at 100 kHz.

4.2. DC-Link Current Ripple—Design of DC-Link Inductor

The decisive parameters for the DC-link inductor are the inductance value L_{dc}, the maximum tolerable peak-to-peak current ripple $\Delta i_{\mathrm{dc\,max}}$, the maximum inductor RMS current $I_{\mathrm{dc\,max}}$, and the maximum inductor peak current $\hat{i}_{\mathrm{dc\,max}}$. Evaluation of the DC-link current ripple is more complex than the output voltage ripple due to the dependence on the rectifier stage configuration (AC-DC or DC-DC) and the characteristics of the load. The current ripple also varies with the shape and phase shift of the output voltages. The subsequent derivations are based on the following simplifications:

- The inverter is supplied by a controlled DC voltage v_{dc} that maintains a constant average DC-link current (excluding the buck stage in the analysis).

- The load is symmetric and the filter capacitors are large enough to minimize voltage ripple, resulting in a purely three-phase sinusoidal output voltage system. This system can be phase-shifted to represent non-unity power factors.

Neglecting converter losses,

$$v_{\mathrm{dc}} \cdot \bar{i}_{\mathrm{dc}} = 3 \cdot V_{\mathrm{ac}} \cdot I_{\mathrm{ac}} \cdot \cos(\varphi) \tag{24}$$

applies where the left side represents the power from the rectifier to the DC-link and the right side represents the average three-phase AC power provided by the inverter stage. Here, v_{dc} represents the ideal (constant) rectifier stage voltage, $\bar{i}_{\mathrm{dc}}$ the ideal constant DC-link current, V_{ac} the RMS value of the three-phase sinusoidal output voltages, I_{ac} the RMS three-phase sinusoidal output current, and $\cos(\varphi)$ the load power factor. Leveraging the previously established current source inverter operation principle ($I_{\mathrm{ac}} = M \cdot \bar{i}_{\mathrm{dc}} \cdot \sqrt{2}$ and $\varphi = \varphi_{\mathrm{v}} - \varphi_{\mathrm{m}}$), the DC-link voltage required to maintain a constant average DC-link current can be derived by

$$v_{\mathrm{dc}} = \frac{3}{\sqrt{2}} \cdot M \cdot V_{\mathrm{ac}} \cdot \cos(\varphi). \tag{25}$$

To compute the DC-link current ripple, the actual switch states for each applied space vector during a PWM period must be considered—e.g., when vector $\underline{\mathrm{I}}_6$ is applied, the voltage across L_{dc} becomes $v_{\mathrm{Ldc}} = V_{\mathrm{DC}} - v_{\mathrm{ab}}$. Each space vector is therefore linked to a line-to-line voltage, such as $V_{\mathrm{V6}} = v_{\mathrm{ab}}$ or $V_{\mathrm{V1}} = -v_{\mathrm{ca}}$. The change in the current during each time interval (t_x, t_y, t_0) of the PWM period can then be calculated for each sector and variant using the relationship

$$\begin{bmatrix} \Delta i_{\mathrm{dc}\,x} \\ \Delta i_{\mathrm{dc}\,y} \\ \Delta i_{\mathrm{dc}\,0} \end{bmatrix} = \frac{1}{L_{\mathrm{dc}}} \cdot \begin{bmatrix} (V_{\mathrm{DC}} - V_{\mathrm{V}x}) \cdot t_x \\ (V_{\mathrm{DC}} - V_{\mathrm{V}y}) \cdot t_y \\ (V_{\mathrm{DC}} - V_{\mathrm{V}z}) \cdot t_0 \end{bmatrix}. \tag{26}$$

This results in, e.g.,

$$\begin{bmatrix} \Delta i_{\mathrm{dc}\,x} \\ \Delta i_{\mathrm{dc}\,y} \\ \Delta i_{\mathrm{dc}\,0} \end{bmatrix} = \frac{T_{\mathrm{pwm}}\, V_{\mathrm{ac}}}{L_{\mathrm{dc}}} \begin{bmatrix} \left(\frac{3}{\sqrt{2}}\, m - \sqrt{6}\, \cos\left(\varphi_{\mathrm{m}} + \frac{\pi}{6}\right)\right) \cdot\, m\, \cos\left(\varphi_{\mathrm{m}} + \frac{\pi}{3}\right) \\ \left(\frac{3}{\sqrt{2}}\, m + \sqrt{6}\, \cos\left(\varphi_{\mathrm{m}} - \frac{3\pi}{6}\right)\right) \cdot\, m\, \cos\left(\varphi_{\mathrm{m}} + \frac{5\pi}{3}\right) \\ \frac{3}{\sqrt{2}}\, m \cdot\, (1 + m\, \cos(\varphi_{\mathrm{m}} + \pi)) \end{bmatrix} \tag{27}$$

for sector Ⅰ with unity power factor ($\cos(\varphi) = 1$). The DC-link current ripple remains the same in all sectors, but is shifted to the sector's center accordingly. The resulting current ripples for modulation indices $M = 1$, $M = 2/3$, and $M = 1/3$ are shown in Figure 11. It is important to note that the DC-link current ripple is independent of the selection of the applied zero space vector. If a symmetric PWM with symmetrical distribution of the applied space vectors is applied, the DC-link current ripple amplitude (peak-to-peak) Δi_{dc} can be obtained by analyzing the PWM sequence for only half of the interval. Similar to the computation of the output voltage ripple, the maximum current ripple for sector Ⅰ with $v_{\mathrm{bc}} > 0$, according to Table 2, can be calculated using

$$\Delta i_{\mathrm{dc}} = \max\left(\frac{\Delta i_{\mathrm{dc}\,x}}{2},\ \Delta i_{\mathrm{dc}\,y},\ \Delta i_{\mathrm{dc}\,0}\right). \tag{28}$$

The ripple amplitude for the PWM scheme summarized in Table 2 is shown in Figure 12 for various modulation indices. Note that only the normalized ripple is presented, and as V_{ac} generally depends on M, the modulation index M affects the amplitudes of the ripple

components. The maximum value of the current ripple $\Delta i_{\mathrm{dc\,max}}$ for $\cos(\varphi) = 1$ can be calculated by carefully analyzing Equation (26) and results in

$$\Delta i_{\mathrm{dc\,max}}(M) = \frac{V_{\mathrm{ac}}\, T_{\mathrm{pwm}}}{L_{\mathrm{dc}}} \left(\frac{3\sqrt{2}}{2} M - \frac{3\sqrt{6}}{4} M^2 \right). \tag{29}$$

The maximum ripple occurs at $M = \frac{1}{\sqrt{3}}$ finally resulting in

$$L_{\mathrm{dc}} = \frac{V_{\mathrm{ac}}\, T_{\mathrm{pwm}}}{\Delta i_{\mathrm{dc\,max}}} \cdot \frac{\sqrt{6}}{4} \tag{30}$$

to estimate the required inductance value L_{dc} of the DC-link inductor. The derived calculation method corresponds to the methods often found in the literature [2,29]. Please note that the current ripple Δi_{dc} can become larger than the value given in Equation (30) for $\cos(\varphi) < 0.83$.

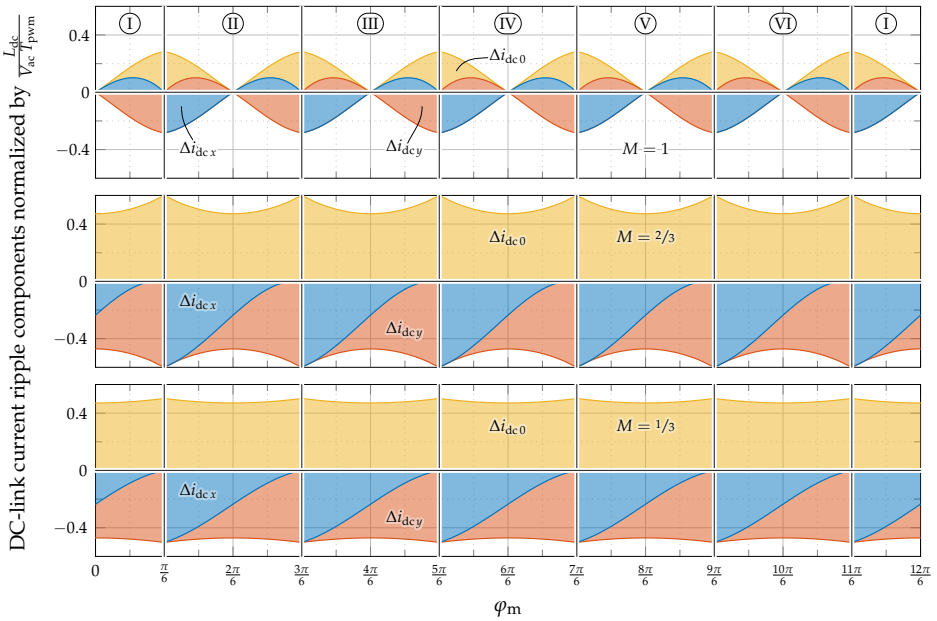

Figure 11. Normalized theoretical DC-link current ripple components $\Delta i_{\mathrm{dc}\,x}$, $\Delta i_{\mathrm{dc}\,y}$, and $\Delta i_{\mathrm{dc}\,0}$ of the CSI if the individual space vectors are applied for their full time intervals in a sequence and not according to the modulation scheme. The three stacked plots represent the components at modulation index $M = 1$, $M = 2/3$, and $M = 1/3$.

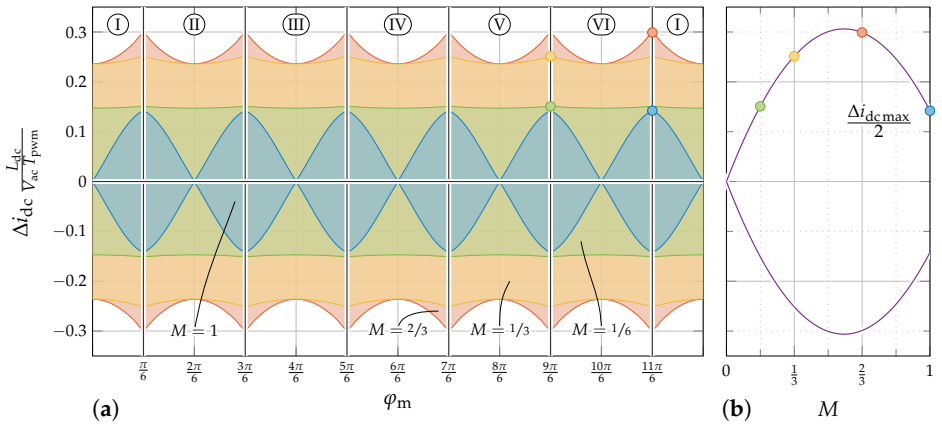

Figure 12. (**a**) Normalized DC-link current ripple amplitude Δi_{dc} at unity power factor for different modulation indices $M = 1$, $2/3$, $1/3$, and $1/6$ and (**b**) resulting peak values of all approaches as a function of modulation index M.

To prevent saturation of the DC-link inductance, the maximum DC-link current $\bar{i}_{\mathrm{dc\,max}}$ is required for the design of the inductor and can be calculated by

$$\bar{i}_{\mathrm{dc\,max}} = \bar{i}_{\mathrm{dc}} + \frac{\Delta i_{\mathrm{dc\,max}}}{2} \tag{31}$$

where $\bar{i}_{\mathrm{dc}}$ is the mean value of the DC-link current and $\Delta i_{\mathrm{dc\,max}}$ is the maximal current ripple given by Equation (30). To estimate winding losses, the RMS value of the DC-link current I_{dc} is required. However, this value cannot be computed analytically anymore, and numerical algorithms are used instead, which are discussed in the following section for the inductor optimization process.

Design of the Inductor

As shown in Figure 1, the DC-link inductor is split into two physical chokes, each with an inductance of $\frac{L_{\mathrm{dc}}}{2}$, to enhance the common mode performance of the circuit. The design method for the DC-link inductors is based on the approach outlined in [32], but has been further improved to better consider the complex DC-link current waveforms appearing in current source inverters.

The design method for the DC-link inductors is based on the approach outlined in [32], which already provides a comprehensive design process and loss modeling method for DC-link inductors based on the worst-case operating points of the CSI for a space vector at one position during standstill. It also greatly simplifies the core loss determination approach by using the standard Steinmetz equation provided in [46,47]. This paper, on the other hand, extends the findings of [32] via a piecewise analysis of the DC-link current waveforms and by using the improved Generalized Steinmetz Equation (iGSE) approach for non-sinusoidal inductor current waveforms in [48–50] and a more realistic consideration of a rotating space vector that yields average inductor core and copper losses. The approach for finding an appropriate winding geometry is also improved in this publication.

The optimization process uses commercially available toroidal core geometries and their specifications. Key geometrical parameters such as the mean magnetic path length l_{m} and the cross-sectional area of the toroid A_{c} are provided by the manufacturer, as well as the differential relative permeability $\mu_{\mathrm{r}}(H)$. The optimization goal of the design process is to minimize both volume and total losses, which include core losses and winding losses.

In this work, high-performance toroidal powder cores from the manufacturer Magnetics (Materials MPP and Edge) are considered. This manufacturer offers analytically fitted equations for the differential relative permeability curve $\mu_{\mathrm{r}}(H)$, as well as the Steinmetz parameters k, α, and β for the different materials and cores. The core geometries include the outer diameter D_{c}, inner diameter d_{c}, height h_{c}, core volume V_{c}, cross-sectional area of the core A_{c}, and mean magnetic path length l_{m}. The design process is carried out numerically for each available core geometry, with outer diameters ranging from 4.19 mm to 167.21 mm, and materials with nominal relative permeability between 14 and 550 are considered.

The initial parameters for the optimization procedure include the PWM frequency f_{pwm}, the average DC-link current $\bar{i}_{\mathrm{dc}}$, the maximum tolerable DC-link current ripple Δi_{dc}, and the maximum RMS output voltage V_{ac} (all from Table 1). The optimization also incorporates copper and core loss estimation, using the analytically derived DC-link current ripple from Figure 12 at different modulation indices, which allows estimating losses at various operating points next to the worst-case operating point regarding inductor losses. As discussed earlier, the current ripple amplitude changes with the output voltage V_{ac} and therefore also with the characteristic of the load. In this work, a linear resistive load is assumed where $V_{\mathrm{ac}} = M \cdot V_{\mathrm{ac\,max}}$, and therefore, the design process depends on the modulation index M. A flow chart of the proposed design process is shown in Figure 13.

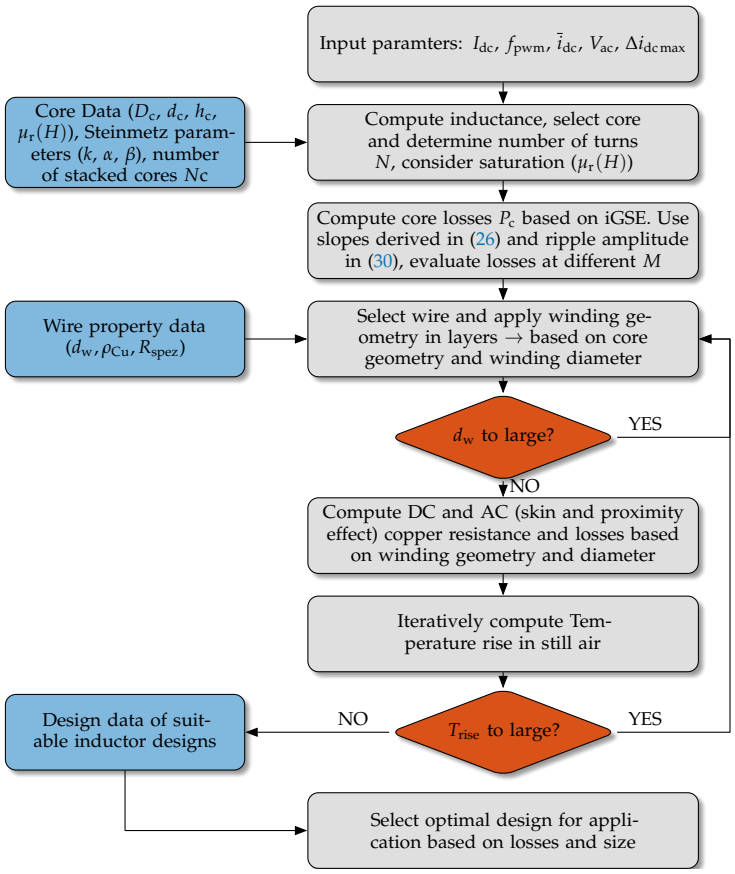

Figure 13. Optimization procedure for DC-link inductor design.

At the beginning of the design process, the relevant input parameters of the converter are collected, including the PWM switching frequency f_{pwm}, the average DC-link current $\bar{i}_{\mathrm{dc}}$, the maximum tolerable DC-link current ripple $\Delta i_{\mathrm{dc\,max}}$, and the maximum RMS output voltage V_{ac}, and the required DC-link inductance can be calculated using Equation (30). Next, a core with specific permeability and geometry is selected from the core database provided by the manufacturer. With the chosen core and the desired inductance value, the number of turns N is determined, accounting for saturation at the given DC-link current. The inductance value of an inductor based on a toroidal power core is given by

$$L = N^2 \cdot \mu_{\mathrm{r}}(H) \cdot \mu_0 \cdot \frac{A_{\mathrm{c}}}{l_{\mathrm{m}}} \tag{32}$$

where A_{c} is the core cross-sectional area and l_{m} is the mean magnetic path length of the toroidal core. The relative permeability μ_{r} depends on the applied DC-field strength, which is caused by the DC-link current in the core, and can be computed using the empirical analytic relationship

$$\mu_{\mathrm{r}}(H) = \frac{0.01 \cdot \mu_{\mathrm{r}}(H=0)}{a + b \cdot \left(\frac{H}{79.5775\,\mathrm{A/m/Oe}}\right)^c} \tag{33}$$

as provided by the manufacturer. Here, c and a are empirical parameters and H is the magnetic field strength in $\mathrm{A\,m^{-1}}$. Note that the actual equation provided has been modified to use SI units. Using the relationship $H(N) = \bar{i}_{\mathrm{dc}} \cdot \frac{N}{l_{\mathrm{m}}}$ in Equation (33) results in

$$1 + \left[100 \cdot b \cdot \left(\frac{\bar{i}_{\mathrm{dc}}}{79.5775\,\mathrm{A/m/Oe} \cdot l_{\mathrm{m}}}\right)^c\right] \cdot N^c - \left[\frac{A_{\mathrm{c}} \cdot \mu_0 \cdot \mu_{\mathrm{r}}(H=0)}{L \cdot l_{\mathrm{m}}}\right] \cdot N^2 = 0, \tag{34}$$

which can now be solved for N. As there is no closed-form analytic solution for N, the number of turns must be determined numerically for each core. After calculating the number of turns, the core losses of the inductor can be estimated. To estimate these losses, the manufacturer provides empirical parameters similar to the Steinmetz parameters

$$P_{\mathrm{mW/cm3}} = a \cdot \hat{B}^{b} \cdot f_{\mathrm{pwm\,kHz}}^{c}, \tag{35}$$

where $P_{\mathrm{mW/cm}}$ represents the core losses in mW cm^{-3}, $\hat{B}$ is the peak value of the flux density in the core, $f_{\mathrm{pwm,kHz}}$ is the PWM frequency in kHz, and a, b, and c are empirical parameters. This equation can then be converted to the standard Steinmetz equation [46,47]

$$P_{\mathrm{fe}} = k \cdot f_{\mathrm{pwm}}^{\alpha} \cdot \hat{B}^{\beta} \tag{36}$$

with parameters $k = \frac{1000 \cdot a}{1000^{c}}$, $\beta = b$, and $\alpha = c$.

As the standard Steinmetz equation is only valid for sinusoidal waveforms, several research groups have developed methods to estimate core losses using the same Steinmetz parameters for non-sinusoidal waveforms [48–50], while [51] showed that the DC-bias has only negligible influence on the losses of the used powder cores. The result of these efforts is the improved Generalized Steinmetz Equation (iGSE):

$$P_{\mathrm{fe}} = \frac{1}{T} \cdot \int_{0}^{T} k_{\mathrm{i}} \cdot \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} \cdot (\Delta B)^{\beta - \alpha} \, \mathrm{d}t. \tag{37}$$

In this context, P_{fe} represents the core losses per period T, $\frac{\mathrm{d}B}{\mathrm{d}t}$ is the rate of change of the flux density during one magnetization period, and ΔB is the peak change in flux density during a cycle. The parameters α and β are the standard Steinmetz parameters. The new parameter k_{i} in the improved Generalized Steinmetz Equation (iGSE) can be computed using

$$k_{\mathrm{i}} = \frac{k}{(2\,\pi)^{\alpha - 1} \int_{0}^{2\,\pi} |\cos\theta|^{\alpha} \, 2^{\beta - \alpha} \, \mathrm{d}\theta}. \tag{38}$$

In a current source inverter, the DC-link current ripple curve changes three times during each PWM interval given by $\Delta i_{\mathrm{dc}\,x}$, $\Delta i_{\mathrm{dc}\,y}$, and $\Delta i_{\mathrm{dc}\,0}$, as shown in Equation (26). These changes depend on the modulation index angle φ_{m} and the modulation index M. The amplitude of the resulting current ripple waveform is then the maximum of the absolute values of the three current changes. Note that for V_{ac} in Equation (26), a linear (resistive) load is assumed, with $V_{\mathrm{ac}} = M \cdot V_{\mathrm{ac,max}}$. Each current ripple component, as well as the total current ripple amplitude, can be converted to corresponding flux density ripples using

$$B = \mu_0 \cdot \mu_{\mathrm{r}}(N, i) \cdot \frac{i \cdot N}{l_{\mathrm{m}}}. \tag{39}$$

To compute the core losses based on the DC-link current waveform of the CSI, the components ΔB and $B(t)$ need to be calculated using the relationship $\mu = \mu_0 \cdot \mu_r$:

$$\Delta B = \frac{\mu\, N}{l_{\mathrm{m}}} \cdot \Delta i_{\mathrm{dc}} \quad \text{and} \quad B(t) = \frac{\mu\, N}{l_{\mathrm{m}}} \cdot i_{\mathrm{dc}}(t). \tag{40}$$

The results can now be used with the iGSE to compute the core losses for one PWM period:

$$\begin{aligned} P_{\mathrm{fe}}(\underline{m}) &= \frac{k_{\mathrm{i}}}{T_{\mathrm{pwm}}} \cdot \left(\frac{\mu N}{l_{\mathrm{m}}} \cdot \Delta i_{\mathrm{dc}} \right)^{\beta-\alpha} \cdot \int_0^{T_{\mathrm{pwm}}} \left| \frac{\mu N}{l_{\mathrm{m}}} \cdot \frac{\mathrm{d}i_{\mathrm{dc}}}{\mathrm{d}t} \right|^{\alpha} \mathrm{d}t \\ &= \frac{k_{\mathrm{i}} \cdot \left(\frac{\mu N}{l_{\mathrm{m}}} \right)^{\beta}}{T_{\mathrm{pwm}}} \cdot \Delta i_{\mathrm{dc}}^{\beta-\alpha} \cdot \left[\left| \frac{\Delta i_{\mathrm{dc}\,0}}{t_0} \right|^{\alpha} \cdot t_0 + \left| \frac{\Delta i_{\mathrm{dc}\,x}}{t_x} \right|^{\alpha} \cdot t_x + \left| \frac{\Delta i_{\mathrm{dc}\,y}}{t_y} \right|^{\alpha} \cdot t_y \right]. \end{aligned} \tag{41}$$

Considering the known symmetry and $\frac{\pi}{3}$-periodicity of the DC-link current ripple at unity power factor, the calculated ripple components from Equation (26) and the time intervals from Equation (8) can be evaluated using Equation (41). The average core loss over a complete electrical period can then be computed through numerical averaging from $\varphi_{\mathrm{m}} = 0$ to $\varphi_{\mathrm{m}} = \frac{\pi}{6}$ for different modulation indices M:

$$P_{\mathrm{fe}}(M) = \frac{6}{\pi} \int_0^{\frac{\pi}{6}} P_{\mathrm{fe}}(\underline{m})\, \mathrm{d}\varphi_{\mathrm{m}}. \tag{42}$$

The maximum occurring core losses for each core are then used as the worst case for the following computations. A loss distribution of inductor losses including core losses is given in Figure 14 as a function of modulation index M for the later designed core based on the design input parameters from Table 1. All acquired parameters of the inductor design process are later summarized in Table 3. Here, the core losses are the averaged core losses over one electrical period. Please note that these are the estimated losses for one of the two designed split inductors.

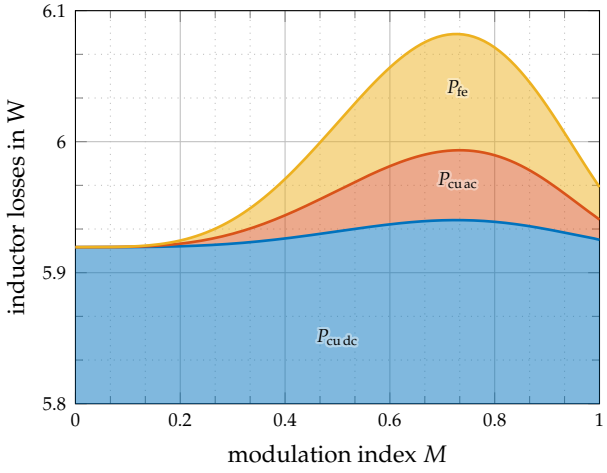

Figure 14. Estimated inductor losses consisting of core losses P_{fe}, DC copper losses $P_{\mathrm{cu\,dc}}$, and AC copper losses $P_{\mathrm{cu\,ac}}$ caused by the high-frequency current ripple for a 583 µH choke, with $N = 51$ turns and the core material "Edge".

The next step in the inductor design process is the selection of the winding arrangement and geometry. A winding arrangement of several layers is used where the number of layers in the inner side of the core and outer side of the core may differ (cf., Figure 15). In this context, k_{i} is the number of layers on the inner side of the core and and k_{o} is the number of layers at the outer side of the core. Also, the number of turns per the inner layer $N_{k,\mathrm{i}}$ may differ from the number of turns at the outer layer $N_{k,\mathrm{o}}$. Please note that the total number of turns on the inner and outer side of the core are equal. To begin this process, a specific wire diameter d_{w} (with the wire radius designated as r_{w}) is selected from a wire diameter database, along with its associated specific resistance R_{spez}. The process is initiated using the largest possible wire diameter.

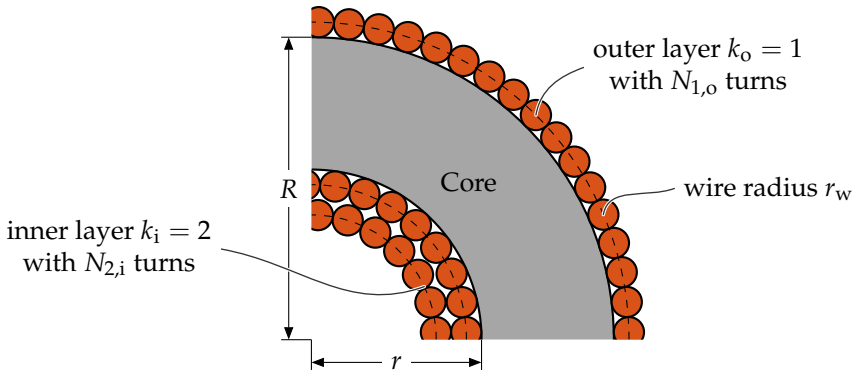

Figure 15. Quarter segment of toroidal core with multi-layer winding arrangement.

This wire diameter is iteratively applied in layers to the inner core section, as shown in Figure 15. The maximum possible inner layer count is $k_{i,max} = \text{floor}\left(\frac{r}{2r_w}\right)$, where r is the inner radius of the core, while the number of applicable turns per inner layer, starting from the innermost layer, is given by $N_{k,i} = \text{floor}\left(\pi/\arcsin\left(\frac{r_w}{r-(2,k_i-1)r_w}\right)\right)$. Therefore, the total number of turns applicable in this way is

$$N_{i\,max} = \sum_{k=1}^{k_{i\,max}} = \text{floor}\left(\frac{\pi}{\arcsin\left(\frac{r_w}{r-(2\,k_i-1)r_w}\right)}\right). \tag{43}$$

If the calculated number of turns exceeds $N_{i,max}$, the design cannot be implemented with the chosen wire diameter, and the process is restarted with the next smaller wire diameter. On the other hand, if $N \leq N_{i,max}$, the required turns are distributed onto the layers starting from the innermost one. The last layer can then be fractionally occupied. A similar winding arrangement strategy is applied at the outer side of the core. Due to the larger outer radius R of the core, the number of turns per outer layer k_o can be calculated as $N_{k\,o} = \text{floor}\left(\pi/\arcsin\left(\frac{r_w}{R+(2\,k_o-1)r_w}\right)\right)$. The total length l_w of the wire

$$\begin{aligned} l_w = & \sum_{k_i=1}^{K_i} N_{k\,i} \cdot (R - r + h + 4\,(2\,k_i - 1)\,r_w) \\ & + \sum_{k_o=1}^{K_o} N_{k\,o} \cdot (R - r + h + 4\,(2\,k_o - 1)\,r_w). \end{aligned} \tag{44}$$

increases per wound inner layer k_i and outer layer k_o by the number of windings applied, i.e., $N_k = N_{k,max}$ for a full layer and potentially less in the last layer.

The inductor volume V_L and the surface area $A_{L,surf}$ can then be calculated using the core's outer dimensions, increased by the winding

$$\begin{aligned} V_L &= D_o^2 \cdot \frac{\pi}{4} \cdot h_o \\ A_{L\,surf} &= \frac{\pi}{2} \cdot \left(D_o^2 - d_i^2\right) + \pi\, h_o \cdot (D_o + d_i) \end{aligned} \tag{45}$$

with the outer diameter $D_o = 2, R + k_o \cdot 4, r_w$, the inner diameter $d_i = 2, r - k_i \cdot 4, r_w$, and the outer height $h_o = h + k_i \cdot 4, r_w$.

The DC resistance of the wire can be determined via $R_{dc} = l_w \cdot R_{spez}$, using the calculated length, where R_{spez} is the specific resistance of the chosen wire per unit length. The DC copper losses can then be calculated by

$$P_{cu\,dc} = \bar{i}_{dc}^2 \cdot R_{dc}. \tag{46}$$

Due to the skin and proximity effects, the AC resistance R_{ac} is increased and needs to be estimated. Therefore, the method proposed in [52,53] is applied as described in [30]. An individual AC resistance can be calculated for each harmonic order n of the non-sinusoidal AC current

$$R_{\mathrm{ac}}^{\langle n \rangle} = R_{\mathrm{dc}} \frac{\gamma}{2} \left[\frac{\mathrm{ber}\,\gamma\,\mathrm{bei}'\,\gamma - \mathrm{bei}\,\gamma\,\mathrm{ber}'\,\gamma}{\mathrm{ber}'^2\gamma + \mathrm{bei}'^2\gamma} - 2\pi\,\eta^2\,\frac{4\,K-1}{3}\,\frac{\mathrm{ber}_2\gamma\,\mathrm{ber}'\gamma + \mathrm{bei}_2\gamma\,\mathrm{bei}'\gamma}{\mathrm{ber}^2\gamma + \mathrm{bei}^2\gamma} \right]. \quad (47)$$

where

$$\begin{aligned} \delta &= \frac{1}{\sqrt{\pi\,n\,f_{\mathrm{pwm}}\,\mu_0\,\frac{1}{\rho_{\mathrm{cu}}}}} \\ \eta &= \frac{d_{\mathrm{w}}}{t}\sqrt{\frac{\pi}{4}} \\ \gamma &= \frac{d_{\mathrm{w}}}{\delta\sqrt{2}} \end{aligned} \quad (48)$$

with the following parameters:

- δ…skin depth
- η…porosity factor
- d_{w}…wire diameter
- n…harmonic order
- f_{pwm}…PWM frequency (fundamental frequency of waveform)
- ρ_{cu}…relative conductivity of copper ($0.017\,86\,\Omega\,\mathrm{mm}^2\,\mathrm{m}^{-1}$)
- t…distance between two adjacent conductors (here, $t = d_{\mathrm{w}}$ was assumed)

The functions "ber" and "bei" represent the Kelvin functions based on the Bessel function of the first kind and order ν, $J_\nu(z)$, where

$$\begin{aligned} \mathrm{ber}_\nu x &= \mathfrak{Re}\left\{ J_\nu\left(x\,\mathrm{e}^{\frac{3\pi i}{4}} \right) \right\} \\ \mathrm{bei}_\nu x &= \mathfrak{Im}\left\{ J_\nu\left(x\,\mathrm{e}^{\frac{3\pi i}{4}} \right) \right\}. \end{aligned} \quad (49)$$

For the zero-order Bessel and Kelvin functions $\nu = 0$, the subscript is not written. The required derivative of the zero-order Kelvin functions can be solved analytically using

$$\begin{aligned} \mathrm{ber}'x &= \frac{\mathrm{bei}_1 x + \mathrm{ber}_1 x}{\sqrt{2}} \\ \mathrm{bei}'x &= \frac{\mathrm{bei}_1 x - \mathrm{ber}_1 x}{\sqrt{2}}. \end{aligned} \quad (50)$$

The harmonic components of the DC-link current (ripple) are computed using a Fourier series analysis, as its shape can be analytically defined by the time intervals t_x, t_y, and t_0 and the corresponding current changes Δi_{dcx}, Δi_{dcy}, and Δi_{dcz}. The general equation for the Fourier series of a periodic signal $x(t)$ is

$$x(t) = a_0 + \sum_{n=1}^{\infty} a_n \cdot \cos(n\,\omega\,t) + b_n \cdot \sin(n\,\omega\,t), \quad (51)$$

where a_0, a_n, and b_n are the Fourier coefficients representing the amplitude of the respective harmonics, and $\omega = \frac{2\pi}{T}$ is the angular frequency corresponding to the fundamental period T. The Fourier coefficients can be computed as follows:

$$
\begin{aligned}
a_0 &= \frac{1}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t)\,\mathrm{d}t \\
a_n &= \frac{2}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t) \cdot \cos(n\,\omega\,t)\,\mathrm{d}t \\
b_n &= \frac{2}{T} \cdot \int_{-\frac{T}{2}}^{\frac{T}{2}} x(t) \cdot \sin(n\,\omega\,t)\,\mathrm{d}t.
\end{aligned} \tag{52}
$$

As i_{dc} is a symmetric and periodic function with a period of $\frac{\pi}{3}$, the Fourier analysis only needs to consider the interval $\varphi_{\mathrm{m}} = 0 \ldots \frac{\pi}{6}$ for the modulation approach discussed in Table 2 for sector Ⅰ. Due to the nature of the current source inverter, the average value of the DC-link current is given by $a_0 = \bar{i}_{\mathrm{dc}}$. The function also exhibits point symmetry around the center of each PWM period, which implies that $a_n = 0$ and only the b_n coefficients are non-zero. The coefficients b_n therefore correspond to the AC current amplitudes at different harmonic orders n. The respective harmonic RMS values concerning Equation (53), given by

$$
I_{\mathrm{dc}}^{\langle n \rangle}(\underline{m}) = \frac{\sqrt{2}}{T_{\mathrm{pwm}}} \cdot \int_{0}^{\frac{T_{\mathrm{pwm}}}{2}} i_{\mathrm{dc}}(t, \underline{m}) \cdot \sin(n\,\omega\,t)\,\mathrm{d}t, \tag{53}
$$

can then be computed by dividing the peak values by $\sqrt{2}$.

The current waveforms can then be defined piecewise

$$
i_{\mathrm{dc}}(t, \underline{m}) = \begin{cases} \frac{\Delta i_{\mathrm{dc}\,0}}{t_0} \cdot t & \forall\ 0 < t < \frac{t_0}{2} \\ \frac{\Delta i_{\mathrm{dc}\,x}}{t_x} \cdot \left(t - \frac{t_0}{2}\right) + \frac{\Delta i_{\mathrm{dc}\,0}}{2} & \forall\ \frac{t_0}{2} < t < \frac{t_0 + t_x}{2} \\ \frac{\Delta i_{\mathrm{dc}\,y}}{t_y} \cdot \left(t - \frac{t_0 + t_x}{2}\right) + \frac{\Delta i_{\mathrm{dc}\,0} + \Delta i_{\mathrm{dc}\,x}}{2} & \forall\ \frac{t_0 + t_x}{2} < t < \frac{T_{\mathrm{pwm}}}{2} \end{cases} \tag{54}
$$

for the different time frames. Please note again that, similar to the derivation of the core losses, V_{ac} in Equation (26) is assumed to change linearly with M!

As analytical solutions for $I_{\mathrm{dc}}^{\langle n \rangle}$ are quite unhandy, especially when considering the functions for the changes in currents and time intervals, they have been solved numerically for a discrete set of modulation indices M and angles φ_{m} during the design process. The corresponding AC copper losses can then be calculated using

$$
P_{\mathrm{cu\,ac}}(\underline{m}) = \sqrt{\sum_{n=1}^{\infty} \left(I_{\mathrm{dc}}^{\langle n \rangle}\right)^2 \cdot R_{\mathrm{ac}}^{\langle n \rangle}}. \tag{55}
$$

To obtain the average losses over one fundamental period, the AC copper losses must be averaged, similar to the core losses. Due to the previously mentioned periodicity and symmetry, this averaging can be performed over a reduced interval.

$$
P_{\mathrm{cu\,ac}}(M) = \frac{6}{\pi} \int_{0}^{\frac{\pi}{6}} P_{\mathrm{cu\,ac}}(\underline{m})\,\mathrm{d}\varphi_{\mathrm{m}} \tag{56}
$$

Once the copper and core losses are determined, the temperature rise T_{rise} can be calculated according to [30] using

$$
T_{\mathrm{rise}} = \left(\frac{P_{\mathrm{fe}} + P_{\mathrm{cu\,ac}} + P_{\mathrm{cu\,dc}}}{10\,A_{\mathrm{L\,surf}}}\right)^{0.833} \tag{57}
$$

where the power variables are given in Watt and surface area is in m^2.

As the increase in the inductor temperature T from its initial value T_0 affects the specific resistivity of the copper ρ_{cu}, both the AC and DC copper resistances are adjusted to the elevated temperature

$$R_{dc}(T = T_0 + T_{rise}) = R_{dc}(T = T_0) \cdot (1 + \alpha\, T_{rise}) \tag{58}$$

considering the specific temperature coefficient of copper of $\alpha = 0.00404\ ^\circ\mathrm{C}^{-1}$. Based on the updated DC resistance at elevated temperature, the corresponding AC and DC copper losses are recalculated using Equations (47) and (56). The resulting temperature rise is then determined using Equation (57). This iterative process continues until the inductor temperature reaches a steady state, i.e., a temperature change below 1% (cf. [30]).

Once an acceptable temperature rise is achieved, the inductor design is complete. Based on the evaluated parameters and the maximum inductor losses, a figure of merit can be calculated for each analyzed core and winding configuration. This figure of merit is essential for optimizing the design. The figure of merit for volume optimization, $\mathrm{FOM_V}$, is given by

$$\mathrm{FOM_V} = V_L \cdot (P_c + P_{cu\,ac} + P_{cu\,dc}). \tag{59}$$

The inductor with the lowest figure of merit is finally chosen from the set of generated designs.

On the basis of the presented optimization process, two optimized split-design inductors have been designed and implemented. The corresponding design input parameters and the specifications of the selected inductor are summarized in Table 3. The loss distribution for the designed inductors at different modulation indices, assuming that V_{ac} varies linearly with M, is presented in Figure 14 as well.

Table 3. Inductor specifications used in this work.

Parameter	Symbol	Value
DC-link current	$\bar{i}_{dc}$	7 A
Nominal output voltage	V_{ac}	200 V
Max. DC-link current ripple	$\Delta i_{dc\,max}$	1.05 A (15% $\bar{i}_{dc}$)
PWM switching frequency	f_{pwm}	100 kHz
DC-link inductance	L_{dc}	$2 \times 583\,\mu$H
Core	-	59894A2 Edge $\mu_r = 60$
Number of stacked cores	N_c	2×3 cores
Number of turns	N	2×51 turns
Wire length	l_w	2×4.59 m
Wire diameter	d_w	1 mm
Max. core losses	$P_{fe\,max}$	2×88.8 mW @ $M = 0.72$
Max. AC copper losses	$P_{cu\,ac\,max}$	2×53.3 mW @ $M = 0.72$
Max. DC copper losses	$P_{cu\,dc\,max}$	2×5.94 W @ $M = 0.72$
Max. temperature rise	$T_{rise\,max}$	45.6 °C @ $M = 0.72$

5. Total Converter Losses

The total losses of the inverter at different load operation points can be determined using the semiconductor switching and conduction losses and the inductor loss distribution. For the following computation, a linear resistive load at the output is assumed.

Using the description of the conduction losses given in Equation (5), the switching losses given in Equation (3) and the DC-link inductor loss components given in Equations (41), (56), and (46) the total converter losses

$$P_{\text{tot}} = P_{\text{c}} + P_{\text{s}} + P_{\text{fe}} + P_{\text{cu dc}} + P_{\text{cu ac}} \tag{60}$$

can be estimated. A total loss summary at different operating points is shown in Figure 16 reassembling the results of Figures 7 and 14 stacked on top of each other.

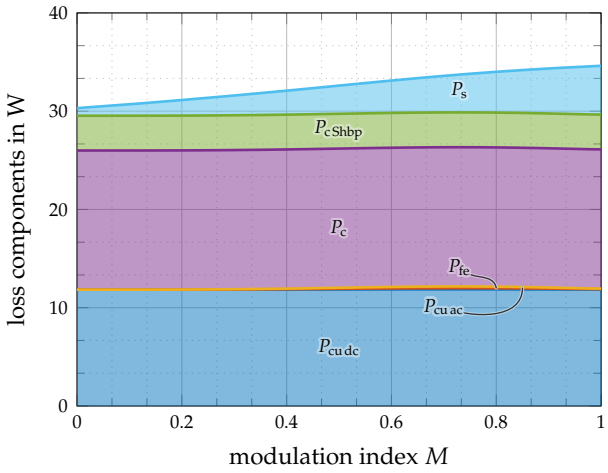

Figure 16. Calculated power losses of the designed current source inverter consisting of power semiconductor conduction losses P_{c} and $P_{\text{c Shb+}}$, switching losses P_{s}, and DC-link inductor losses $P_{\text{cu dc}}$, with $P_{\text{cu ac}}$ and P_{fe} as a function of modulation index M for $\bar{i}_{\text{dc}} = 7$ A. A constant resistive load is assumed, lowering V_{ac} linearly towards lower modulation indices.

It can be observed that the conduction losses, consisting of power semiconductor conduction losses and AC and DC copper losses in the DC-link inductors of the presented current source inverter design, dominate the estimated total losses. Due to the constant DC-link current, these losses, neglecting the heating of the current-carrying components, are approximately constant over the entire load range of a resistive load. As expected, the switching losses increase linearly with increasing modulation index and therefore with increasing output voltage. However, even at nominal load, these only make up a small proportion of the total losses. In this case, the circuit would benefit from the selection of optimized semiconductor switches with lower on-resistance, which could reduce the conduction losses at the expense of higher switching losses. Furthermore, as shown in [54], the performance of the inverter could be greatly improved in the partial load operation by reducing the DC-link current at lower modulation indices.

6. Experimental Verification

Based on the proposed design process and loss modeling method, a laboratory CSI prototype has been designed and manufactured which is used to experimentally verify the theoretical findings. It consists of a three-phase CSI output stage for motor drives and includes a buck input stage for operation from a DC voltage source, such as a battery or a fuel cell. The constructed circuit is derived from the schematic representation provided in Figure 1. The included buck stage was, however, not within the scope of this investigation and has been deactivated during the experiments by turning on $S_{\text{HB+}}$ constantly, and the required input voltage V_{dc} was generated directly using a laboratory power supply. Figure 17 presents an image of the developed CSI hardware laboratory prototype, which features a compact, stacked two-board design with two split inductors, an integrated heat sink, and fans.

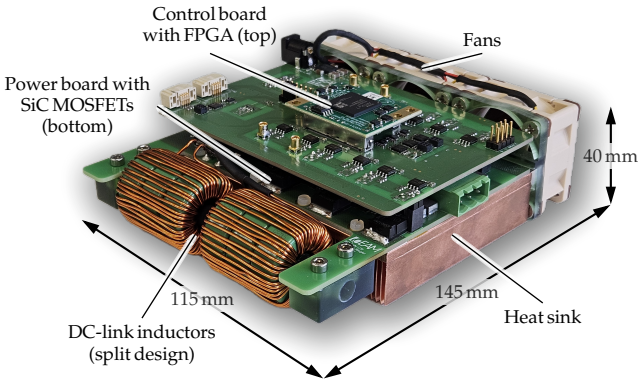

Figure 17. Prototype of the implemented buck-CSI system showcasing a compact, stacked two-board design with an integrated thermal management system and two (split) DC-link inductors.

The top board of the prototype accommodates an FPGA-based control platform running a custom control scheme and computing the space vector modulation algorithm, with ADCs for output along with DC-link current and voltage measurement, and includes the driver circuits and isolated gate drive power supply for the SiC MOSFETs. The bottom board contains the power circuit with the SiC MOSFETs along with the filter capacitors, optimized for thermal and electrical performance. An integrated thermal management system for the power semiconductor switches consisting of a copper heat sink and three axial fans, as already mentioned in Section 3.2, is located underneath the bottom board. The total volume of the converter including buck stage (not in operation) with a length of 145 mm, width of 115 mm, and height of 40 mm is 0.667 L, resulting in a volumetric converter power density of 4.5 kW/L. The reverse voltage blocking capability of the main switching elements was achieved using a common source back-to-back configuration of two SiC-based MOSFETs (IMBG65R072M1H) in a small-footprint SMD package (TO-263-7). For the DC-link inductor L_{dc}, a split toroidal inductor was prototyped according to the design results in Section 4.2 and implemented as shown in Figure 1. The filter capacitors are ceramic capacitors based on C0G material that are placed as close as possible to the semiconductor switches, further minimizing the area of the commutation loop and decreasing switching losses.

The nominal AC output power of the converter is $P_{ac} = 3\,\text{kW}$, with a maximum RMS output voltage of $V_{ac} = 200\,\text{V}$, resulting in an average DC-link current of $\bar{i}_{dc} = 7\,\text{A}$. The maximum DC input voltage of the system is $V_{dc} = 500\,\text{V}$. The initial PWM carrier frequency was chosen to be $f_{pwm} = 100\,\text{kHz}$ for the CSI. Table 4 provides a detailed summary of the prototype specifications. Please note that for all experiments, the inverter stage was operated in open-loop control.

Table 4. Summary of the prototype specifications.

Parameter	Symbol	Value
Nominal output power	P_{ac}	3 kW
Nominal output voltage	V_{ac}	200 V
Nominal output current	I_{ac}	5 A
DC-link current	$\bar{i}_{dc}$	7 A
Maximum DC-link voltage	V_{dc}	500 V
PWM switching frequency	f_{pwm}	100 kHz
DC-link inductance	L_{dc}	$2 \times 583\,\mu\text{H}$ (51 turns on 3 cores, $\mu_r = 60$)
Filter capacitance	C_f	$8 \times 100\,\text{nF}$ (C0G in 2220 package)
Power semiconductor	-	IMBG65R072M1H
CSI overlap time	t_{ol}	30 ns
Converter dimensions	-	145 mm × 115 mm × 40 mm
Converter volume	V_{CSI}	0.667 L
Volumetric power density	$\rho_{V\,CSI}$	4.5 kW/L

Experimental Results

The theoretical results for the AC voltage waveforms of Section 4.1, the DC-link current waveform of Section 4.2, and the converter loss modeling from Section 5 were experimentally verified using the implemented prototype. The converter efficiency was measured over the entire rated load range of the converter and the inverter output voltages and DC-link voltages and currents were recorded accordingly.

The following procedure was applied for this measurement:

- The inverter was loaded with three resistors of $R_l = 40\,\Omega$, which behaves like the linear load as assumed during the design process, ensuring the rated output voltage of $V_{ac} = 200\,\text{V}$ at $M = 1$ and $\bar{i}_{dc} = 7\,\text{A}$.
- The average DC-link current was maintained constant at 7 A with an appropriate DC power supply in constant current mode at the input.
- The PWM frequency was set to 100 kHz, the AC output frequency to 100 Hz (period 10 ms), and the modulation index was decreased in steps from $M = 1$ to $M = 0.1$ to reduce the output power from the nominal operating point.
- The DC-link current i_{dc}, the input voltage V_{dc}, the three output currents i_a, i_b, and i_c, as well as the line-to-line output voltages v_{ab}, v_{bc}, and v_{ca} were measured using an oscilloscope (*Tektronix 5 Series*) with appropriate current clamps and differential voltage probes, resulting in a total measurement bandwidth of 50 MHz. The phase voltage quantities v_a, v_b, and v_c were subsequently calculated from the measured line-to-line voltages via $v_a = \frac{v_{ab} - v_{ca}}{3}$, $v_b = \frac{v_{bc} - v_{ab}}{3}$, and $v_c = \frac{v_{ca} - v_{bc}}{3}$ to be able to compare the measurement results with the analytical derivations for the phase voltage ripple.
- The converter efficiency was measured using a *HIOKI PW8001* power analyzer employing *HIOKI U7005* current transducers.

The measured current and voltage waveforms for an output power of $P_{ac} = 2\,\text{kW}$ ($^2/_3$ of the nominal load) are shown in Figure 18 for a modulation index of $M = 0.817$. Please note that the phase voltages were calculated from the measured line-to-line voltages.

Figure 19 additionally shows the output voltage ripple in phase a and the DC-link current ripple for the same operating point at an output power of $P_{ac} = 2\,\text{kW}$. The output voltage ripple was obtained by appropriate high-pass filtering of the measured v_a and the ripple of the DC-link current was obtained by subtracting the average DC-link current. Both Figure 19a,b additionally show zoomed subplots of the respective waveforms to highlight the individual voltage and current slopes at sector Ⅵ (at −2 ms) and sector Ⅲ (at 4 ms).

The output voltage ripple for sector Ⅵ (left zoomed plot) shows that v_a increases during time intervals $t_y/2$ and decreases in intervals $t_0/2$ and t_x, which corresponds to the signs of the curves displayed in Figure 9. The corresponding sequencing $t_0/2 \rightarrow t_y/2 \rightarrow t_x \rightarrow t_y/2 \rightarrow t_0/2$ then results in a reduced amplitude for the output voltage ripple. In contrast, the sequence for sector Ⅲ (right zoomed plot) is selected in such a way that the two intervals t_x and t_y in which the voltage increases are directly adjacent in the center of the interval. This results in a higher ripple amplitude over the entire PWM period. The total measured envelope of the voltage ripple is in good agreement with the theoretical curves of Figure 10.

As illustrated previously in Figure 12, the sequencing of separate sub-intervals does not result in a decrease in DC-link current ripple amplitude. As anticipated, the observed ripple envelope shows periodicity with the sectors; however, there are slight differences in shape between even and odd sectors. The overshoots observed in the current result from the parasitic winding capacitance associated with the DC-link inductors. The measured current ripple amplitudes again agree well with the theoretical values in Figure 12.

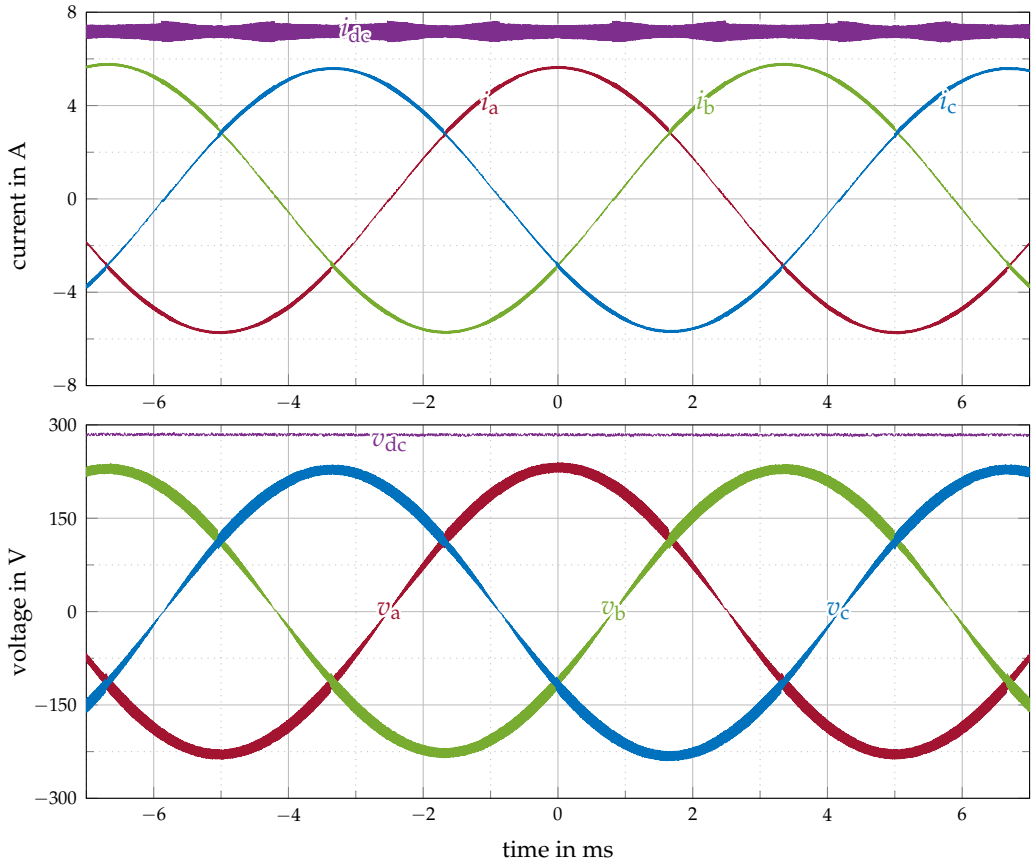

Figure 18. Measured voltage and current waveforms (Tektronix 5 Series, measurement bandwidth 50 MHz) at an operating point of $\bar{i}_{dc} = 7\,\text{A}$, $f_{pwm} = 100\,\text{kHz}$, $P_{ac} = 2\,\text{kW}$, and $R_l = 40\,\Omega$ ($\hat{i}_{ac} \sim 5.8\,\text{A}$). All waveforms have been filtered with a first-order low-pass with a cutoff frequency of $f_c = 1\,\text{MHz}$ to filter out switching noise and to better visualize the resulting waveforms.

Figure 20 presents the efficiency of the converter η_{meas} as measured by the power analyzer across seven distinct operating points and corresponding modulation indices. Throughout the entirety of the measurement process, the DC-link current was maintained at 7 A by utilizing a DC power supply. The measurement points are denoted by black dots and interpolated using a dashed line to emphasize the converter efficiency curve across various operating points for a constant load.

In addition to the measured results, the theoretically calculated efficiencies for each loss component analyzed in the preceding sections are displayed as colored areas. The efficiency areas are calculated by taking the semiconductor switching losses P_s, conduction losses P_c and $P_{c\,Shbp}$, inductor core losses P_{fe}, and inductor DC and AC copper losses $P_{cu\,dc}$ and $P_{cu\,ac}$ from Figure 16 and converting them into the respective efficiency curves via $\eta = \frac{P_{ac}}{P_{ac}+P}$. Here, the modulation index dependent converter AC output power corresponds to $P_{ac} = 3\,\text{kW}\cdot\text{M}^2$. The efficiency of the converter reaches its maximum at approximately 98.8% at the nominal operating point of $P_{ac} = 3\,\text{kW}$. As the output power decreases, the efficiency decreases, but maintains a value of 97.9% at 1.5 kW.

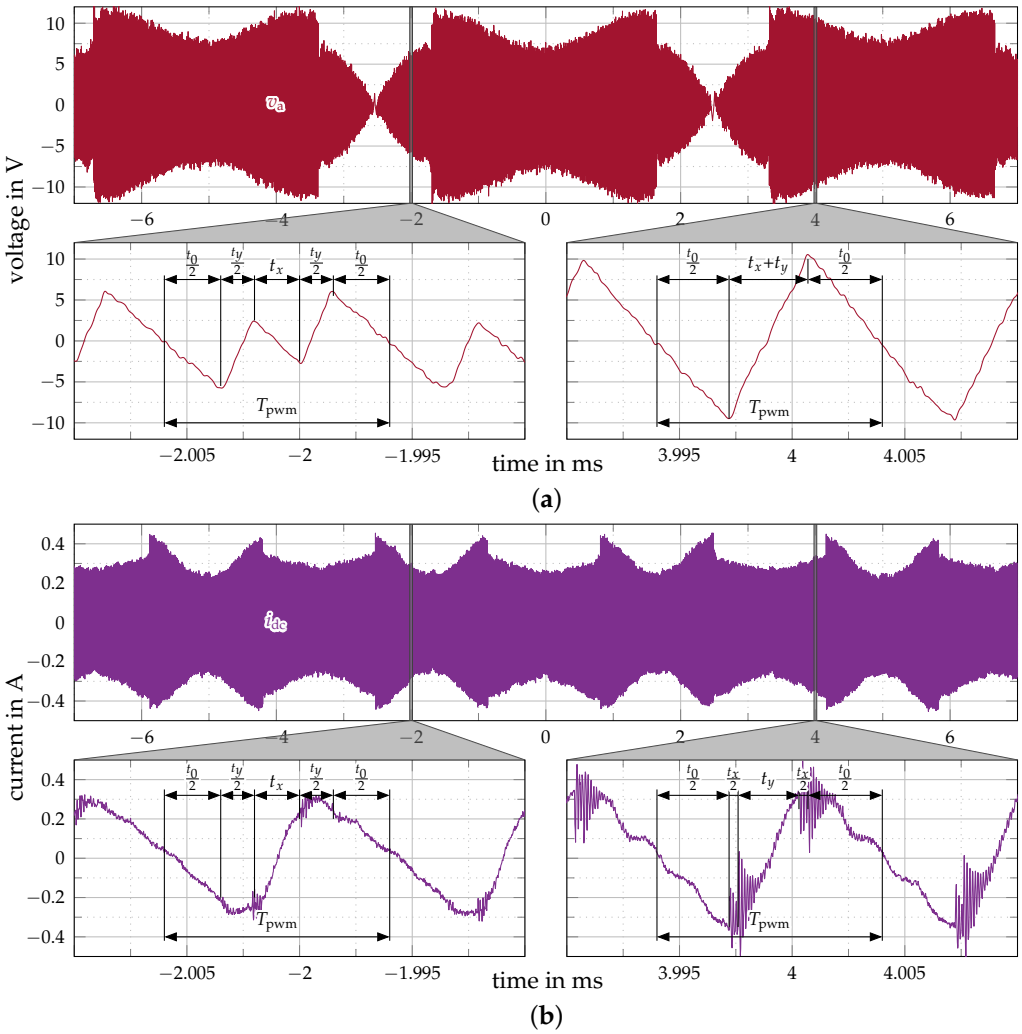

Figure 19. (**a**) Measured (Tektronix 5 Series, measurement bandwidth 50 MHz) output voltage ripple of phase a and (**b**) measured DC-link current ripple at operating point $\bar{i}_{dc} = 7\,A$, $f_{pwm} = 100\,kHz$, $P_{ac} = 2\,kW$, and $R_l = 40\,\Omega$ ($\hat{i}_{ac} \sim 5.8\,A$) including zoomed subplots for sector (VI) (at $-2\,ms$) and sector (III) (at $4\,ms$). All waveforms have been filtered with a first-order low-pass with a cutoff frequency of $f_c = 1\,MHz$.

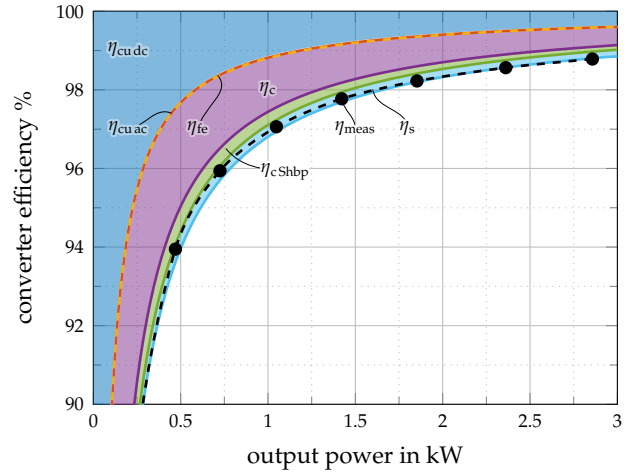

Figure 20. Measured efficiency curve (black dots, HIOKI PW8001) of the implemented converter at different modulation indices resulting in different AC output powers at $i_{dc} = 7\,A$ and $f_{pwm} = 100\,kHz$ for a constant load of $R_l = 40\,\Omega$ per phase.

Additionally, the efficiency calculated using the loss separation method from the preceding sections is in excellent agreement with the efficiency measured by the power analyzer, which provides strong evidence that the proposed design approach for CSIs is viable.

7. Conclusions

This paper presents a comprehensive framework for the design and analysis of silicon-carbide semiconductor-based current source inverters (CSIs) for high-performance motor drive applications. The proposed methodology integrates analytic and numerical techniques to optimize passive component design, including filter capacitors and the DC-link inductor, and provides comprehensive efficiency estimation for semiconductor switching losses and conduction losses, as well as for losses occurring in the DC-link inductor. A laboratory hardware prototype CSI with the specifications given in Table 1 is developed, built, and tested. The theoretical findings based on analytical models are then compared to the experimental results taken from the constructed hardware prototype. The efficiency calculated using the loss separation method from the preceding sections, as well as the analytically derived current and voltage ripple waveforms, is in excellent agreement with measured results, providing strong evidence that the presented design approach for CSIs is viable.

Author Contributions: Conceptualization, methodology, software, validation, formal analysis, investigation, data curation, writing—original draft preparation, and visualization: B.R.; resources, writing—review and editing, supervision, project administration, and funding acquisition: M.H. All authors have read and agreed to the published version of the manuscript.

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Abbreviations

The following abbreviations are used in this manuscript:

MDPI	Multidisciplinary Digital Publishing Institute
CSI	Current source inverter
CSC	Current source converter
BD	Bidirectional
RVB	Reverse voltage blocking
FPGA	Field Programmable Gate Array
ADC	Analog to Digital Converter
PWM	Pulse Width Modulation
RVM	Reduced Voltage Modulation
SiC	Silicon Carbide
GaN	Gallium Nitride

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