Efficiency Considerations of a 3 kW, all SiC Current-Source Converter

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***Abstract*—Current source inverters (CSIs) offer an interesting alternative to classical voltage source inverters (VSI) in drive applications due to their smooth output characteristics. This work discusses a three-phase CSI powered by a DC source, such as a battery or fuel cell, in detail. The CSI is connected to the DC-source using a single buck-stage able to control the DC-link current of the CSI. The two converter stages provide flexibility in managing the DC-link current magnitude and modulation index, resulting in three meaningful operating modes. While for two operating modes either the DC-link current or the modulation index is kept constant in the third operating mode a 2/3 PWM approach is chosen. These three operating modes are analyzed in detail, and theoretical results are validated through experimental tests on a constructed ultra-compact, high-efficiency, all-SiC three-phase CSI laboratory prototype with a switching frequency of up to 200 kHz.**

***Index Terms*—Current-source converter, current-source inverter, wide-bandgap semiconductor, high switching frequency**

I. Introduction

The use of wide-bandgap (WBG) semiconductor switches (SiC, GaN), enables a significant increase in switching frequencies of power electronic converters used in electric drives. In addition, these new devices offer lower conduction losses and are better suited for high temperature operation [1]–[3]. However, in conventional voltage-source inverters (VSI), increasing the switching frequency reduces the size of the passive components, but, due to higher $^{dv}/_{dt}$ during switching in the case of WBG devices, it also implies increased EMI issues, overvoltage at the motor terminals, and leads to additional losses in the electric machine [4].

One possible solution to overcome such challenges is to replace the conventional VSI with the dual current source-inverter (CSI) topology [4], [5]. That is thanks to the inherent filtering of the output quantities provided by the CSI topology. The circuit diagram of a three-phase CSI supplied by a buck-stage from a DC source is depicted in **Fig. 1**. The main energy storage element in the DC-link is the inductor L_{dc} by which, with appropriate control of the input buck-stage, the DC-link current i_{dc} is kept constant on average. This current can then be applied to the load using suitable PWM control of the inverter to generate arbitrary three-phase current waveforms i_a, i_b, and i_c. The capacitors C_f provide filtering of the output voltage, eliminating the need for an additional output filter. Due to the inherent boost capability of the CSI, this topology can be advantageously combined with an input buck-type stage to achieve a higher output voltage range than that of VSIs alone. The filter inductance required for the single-phase buck-stage can be implemented as a shared component with the CSI, as illustrated in **Fig. 1** [4].

In the CSI, the semiconductor switches must be able to block voltages in reverse-direction (RB) and able to conduct current in a single direction to avoid potentially

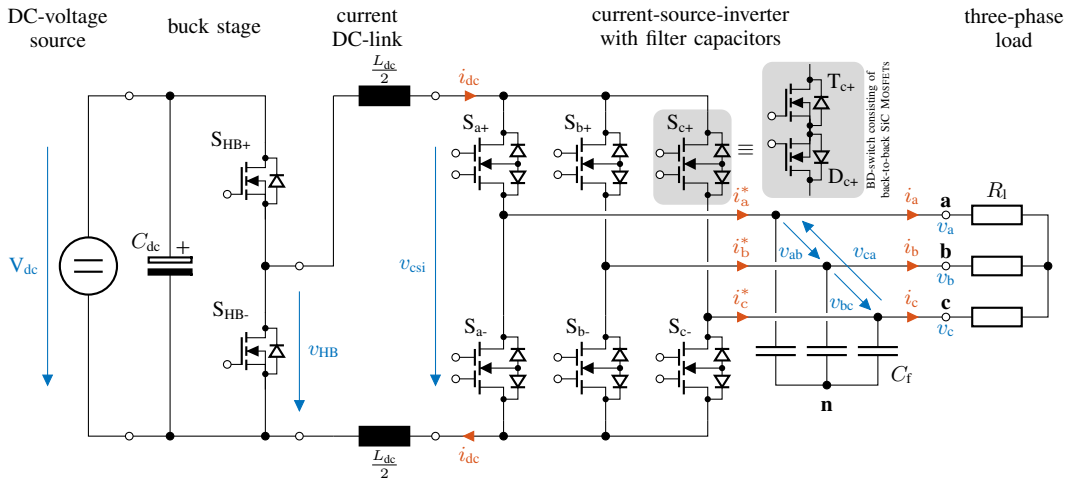


Fig. 1. Basic circuit diagram of the CSI with a buck-stage input connected to a three-phase resistive load R_l. The reverse-blocking semiconductor switches are represented by MOSFETs arranged in a back-to-back (common source) configuration, and the DC-link inductor is split between the positive and negative rails.

destructive short- and open-circuit events during the commutations. To build switches with RB capability using available components, a conventional reverse-conducting switch can be combined with a diode in series, or using another switch in back-to-back arrangement, as in the presented prototype, to further lower conduction losses compared to using a diode. Due to the HEMT structure of currently available GaN switches monolithic integrated switches can be implemented [6]–[8]. This is, however, not possible using switches based on SiC (vertical technology) and a custom implementation as discussed above must be pursued.

II. Theory of Operation

In order to output an arbitrary three-phase current at the output of the inverter stage, space-vector-modulation (SVM) is used. In contrast to the VSI topology, the CSI structure consists of only two fundamental building blocks: the upper three-way switch formed by S_{a+}, S_{b+}, and S_{c+} and the lower three-way switch consisting of S_{a-}, S_{b-}, and S_{c-}. The permissible states for these switches are that, except during commutations, only one upper and one lower switch are turned on at any given time, to conduct the DC-link current.

This results in a total of nine possible switching states. six of them active states, meaning that they result in a non-zero current flow of i_a^*, i_b^*, or i_c^* (e.g. when S_{a+} and S_{b-} are turned on). The remaining three are zero (or freewheeling) states, where the upper and lower switch of the same phase are turned on resulting in zero current flow for i_a^*, i_b^*, or i_c^* (e.g. when S_{a+} and S_{a-} are turned on). The respective current of each state can then be transformed into the complex current space vector $\underline{i}^*$ via the transformation $\underline{i}^* = \frac{2}{3}\left[1\ \mathrm{e}^{\mathrm{j}\frac{-2\pi}{3}}\ \mathrm{e}^{\mathrm{j}\frac{2\pi}{3}}\right] \cdot \left[i_a^*\ i_b^*\ i_c^*\right]^{\mathrm{T}}$.

The complex representations of the 9 different states ($\underline{i}_1^* \dots \underline{i}_9^*$) of the CSI are then normalized (divided by) the average DC-link current $\bar{i}_{dc}$, resulting in 9 space vectors $\underline{\mathrm{I}}_1 \dots \underline{\mathrm{I}}_9$. A graphical representation of the space vectors is shown in the space vector diagram in **Fig. 2**.

The 6 space vectors of the active states divide the complex plane into 6 sectors Ⅰ…Ⅵ, where each sector is bounded by 2 space vectors (e.g. sector Ⅰ is bounded by $\underline{\mathrm{I}}_6$ and $\underline{\mathrm{I}}_1$). An arbitrary space vector $\underline{m} = M\,\mathrm{e}^{\mathrm{j}\,\varphi_m}$ can then be synthesized in a PWM scheme by a linear combination of the two vectors bounding the respective sector in which the desired space vector is located. In the PWM scheme, during one switching period T_{pwm}, the two states representing the bounding space vectors and one arbitrarily selectable zero state are applied for a certain time each (These time intervals are denoted by t_1, t_6, and t_7 in **Fig. 2**). Please note that the sequence each vector is applied within one PWM period has an impact on switching losses, DC-link current ripple, output voltage ripple, and common mode voltage.

The resulting output current can be computed by multiplying $\underline{m}$ by the currently applied DC-link current, $\underline{\bar{i}}^* = \bar{i}_{dc} \cdot \underline{m}$. A locally averaged three-phase sinusoidal output current is generated by rotating $\underline{m}$ at a certain angular speed. Since the high-frequency AC component of $\underline{i}^*$ is filtered by the filter capacitors, the averaged currents at the switch nodes correspond to the output current of the inverter $\left(\underline{\bar{i}}^* = \underline{i} \rightarrow \left[i_a\ i_b\ i_c\right]\right)$.

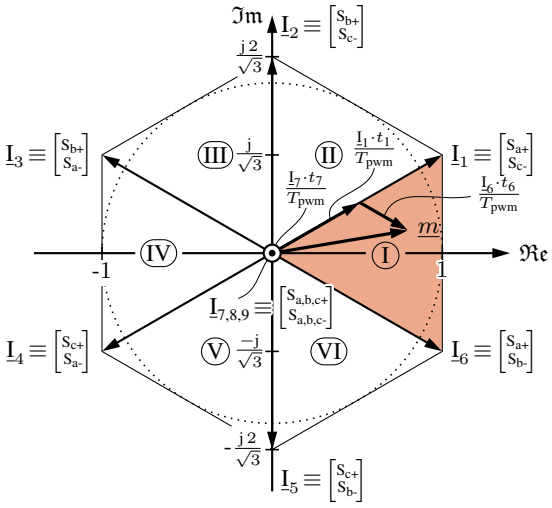


Fig. 2. Space Vector Diagram for the CSI with 6 active ($\underline{\mathrm{I}}_1 \dots \underline{\mathrm{I}}_6$) and three zero space vectors ($\underline{\mathrm{I}}_7 \dots \underline{\mathrm{I}}_9$) dividing the complex plane into a hexagon with 6 sectors $\left(\text{Ⅰ} \dots \text{Ⅵ}\right)$.

III. Simplified Switching Loss Model

Due to the switching actions of the three-way switches switching losses occur also in the CSI. To quantify and compare the occurring switching losses across different modes of operation and modulation strategies a simplified loss model is introduced. This model is derived from the measured losses in a commutation cell, as detailed in [9]. A brief summary of these findings is shown in **Fig. 3**. The switching losses can be determined by measuring voltages across- and currents through each semiconductor switch. The commutation current i_c corresponds to the DC-link current i_{dc}, while the commutation voltage v_c represents the respective line-to-line output voltage (v_{ab}, v_{bc}, or v_{ca}) across the capacitor.

Based on the measured results the switching losses can be approximated by a linear dependency on switch voltage and current. However, it should be noted that this linearization tends to overestimate the hard-switching losses. Additionally, if the commutation voltage is negative during a commutation event, the respective transition is classified as a soft-switching transition (indicated by $\rightarrow$). Conversely, if the commutation voltage is positive, the transition is classified as hard-switching (indicated by $\Rightarrow$). Under these assumptions, a simplified switching loss model according to (1) is proposed.

$$E_s(v_c, i_c) = \begin{cases} E_{soft} = k_{soft}\, v_c\, i_c \ \forall\ {}^{v_c<0\,\&\,i_c\geq 0}_{v_c\geq 0\,\&\,i_c<0} \\ E_{hard} = k_{hard}\, v_c\, i_c \ \forall\ {}^{v_c\geq 0\,\&\,i_c\geq 0}_{v_c<\,\&\,i_c<0} \end{cases} \tag{1}$$

Here, E_s denotes the sum of the switching energy occurring in all involved devices during one switching event, and the two constants k_{hard} and k_{soft} describe the linear

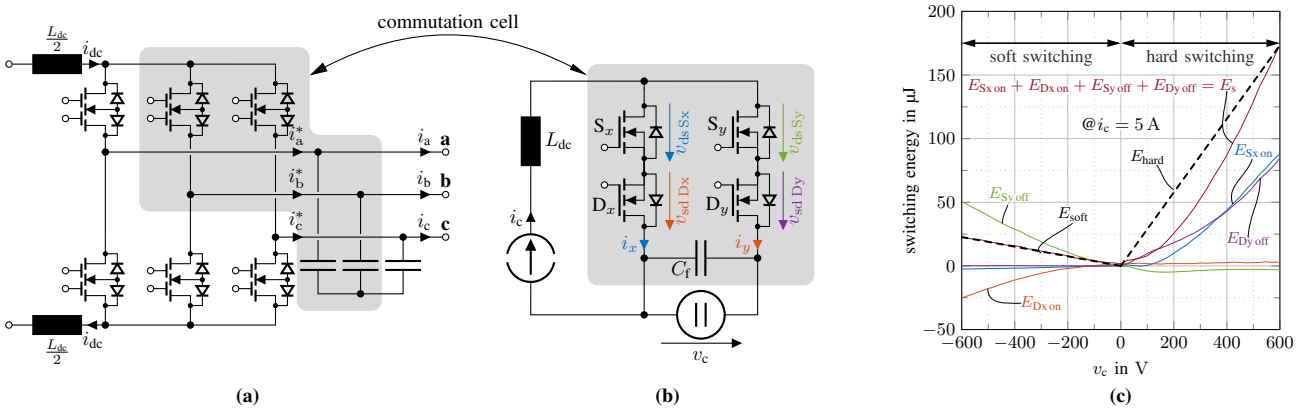


Fig. 3. Switching loss measurement for CSIs. **(a)** Basic circuit diagram of the CSI. **(b)** Commutation cell derived from the CSI. **(c)** Switching energies as a function of commutation voltage for a commutation from S_x/D_x to S_y/D_y.

relationship of the switching losses with respect to commutation current i_c and voltage v_c. Please note that this switching loss model focuses only on the two switching elements involved in one commutation. It neglects the losses caused by the voltage change in the third switch (see [7]) due to the presence of a three-phase voltage system at the inverter output and the resulting possible distribution of the line-to-line voltage across the active switch and reverse blocking device.

The total switching losses also depend on the commutation sequence used. The objective of the modulation scheme is to minimize switching losses and DC-link current ripple to allow for the smallest possible DC-link inductor design. Previous studies, such as [10]–[13], have compared different modulation schemes regarding their switching losses. They found that the strategy referred to as Modified Fullwave Symmetrical Modulation (MFSM) yields the lowest switching losses among all modulation strategies.

Tab. I summarizes the turn-on and -off sequences of the inverters semiconductor switches during one PWM period for each sector, based on the polarities of the line-to-line output voltages. The voltages above the arrows indicating one commutation event denote the respective commutation voltage v_c according to (1). A positive commutation voltage, resulting in a hard-switching event ($\Rightarrow$) is indicated using red color and a negative commutation voltage resulting in a soft-switching event ($\rightarrow$). It should be noted that for switching actions between the upper switches of the CSI, the commutation current equals the DC-link current. For switching actions between the lower switches, it equals the negative DC-link current, thus inverting the soft- and hard-switching behavior. **Fig. 4** depicts a set of expected line-to-line output voltage waveforms at unity power factor, highlighting the corresponding voltages for hard- and soft-switching in sector (II). Note that at unity power factor, the voltage condition ($v_{ab} > 0$ or $v_{ab} < 0$) for selecting the sequence changes in the midpoint of the sector. Consequently, for MFSM, the respective line-to-line voltage with the highest amplitude is never involved in a commutation event.

IV. Modes of Operation

The system at hand consists of two converter stages: a buck-stage and a three-phase current source inverter stage. This configuration provides a degree of freedom, allowing for different operating modes of the converter system. In this work, three distinct operating modes are analyzed in detail and compared. These have the following basic characteristics.

Table I

Swithing cycles of the reverse blocking semiconductor switches during one PWM period for the MFSM modulation strategy and 2/3 modulation strategy [14], [15] method in sectors (I), (II), and (III). Soft-switching transitions are indicated by a single ($\rightarrow$), while hard-switching transitions denoted by a double-stroke arrow ($\Rightarrow$) [15]

Sector	Condition	Switching Cycle MFSM (• $v_c > 0$), • $v_c < 0$)	Switching Cycle 2/3 PWM (• $v_c > 0$), • $v_c < 0$)
(I)	$v_{bc} < 0$	$\begin{bmatrix}S_{a+}\\S_{a-}\end{bmatrix} \xrightarrow{-v_{ca}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xrightarrow{-v_{bc}} \begin{bmatrix}S_{a+}\\S_{b-}\end{bmatrix} \xRightarrow{v_{bc}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{ca}} \begin{bmatrix}S_{a+}\\S_{a-}\end{bmatrix}$	$\begin{bmatrix}S_{a+}\\S_{b-}\end{bmatrix} \xRightarrow{v_{bc}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xrightarrow{-v_{bc}} \begin{bmatrix}S_{a+}\\S_{b-}\end{bmatrix}$
	$v_{bc} > 0$	$\begin{bmatrix}S_{a+}\\S_{a-}\end{bmatrix} \xrightarrow{v_{ab}} \begin{bmatrix}S_{a+}\\S_{b-}\end{bmatrix} \xrightarrow{v_{bc}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xRightarrow{-v_{bc}} \begin{bmatrix}S_{a+}\\S_{b-}\end{bmatrix} \xRightarrow{-v_{ab}} \begin{bmatrix}S_{a+}\\S_{a-}\end{bmatrix}$	$\begin{bmatrix}S_{a+}\\S_{b-}\end{bmatrix} \xRightarrow{v_{bc}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xRightarrow{-v_{bc}} \begin{bmatrix}S_{a+}\\S_{b-}\end{bmatrix}$
(II)	$v_{ab} > 0$	$\begin{bmatrix}S_{c+}\\S_{c-}\end{bmatrix} \xrightarrow{-v_{bc}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xrightarrow{-v_{ab}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{ab}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{bc}} \begin{bmatrix}S_{c+}\\S_{c-}\end{bmatrix}$	$\begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{ab}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xrightarrow{-v_{ab}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix}$
	$v_{ab} < 0$	$\begin{bmatrix}S_{c+}\\S_{c-}\end{bmatrix} \xrightarrow{v_{ca}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xrightarrow{v_{ab}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xRightarrow{-v_{ab}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xRightarrow{-v_{ca}} \begin{bmatrix}S_{c+}\\S_{c-}\end{bmatrix}$	$\begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{ab}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xRightarrow{-v_{ab}} \begin{bmatrix}S_{a+}\\S_{c-}\end{bmatrix}$
(III)	$v_{ca} < 0$	$\begin{bmatrix}S_{b+}\\S_{b-}\end{bmatrix} \xrightarrow{-v_{ab}} \begin{bmatrix}S_{b+}\\S_{a-}\end{bmatrix} \xrightarrow{-v_{ca}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{ca}} \begin{bmatrix}S_{b+}\\S_{a-}\end{bmatrix} \xRightarrow{v_{ab}} \begin{bmatrix}S_{b+}\\S_{b-}\end{bmatrix}$	$\begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{ca}} \begin{bmatrix}S_{b+}\\S_{a-}\end{bmatrix} \xrightarrow{-v_{ca}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix}$
	$v_{ca} > 0$	$\begin{bmatrix}S_{b+}\\S_{b-}\end{bmatrix} \xrightarrow{v_{bc}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xrightarrow{v_{ca}} \begin{bmatrix}S_{b+}\\S_{a-}\end{bmatrix} \xRightarrow{-v_{ca}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xRightarrow{-v_{bc}} \begin{bmatrix}S_{b+}\\S_{b-}\end{bmatrix}$	$\begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix} \xRightarrow{v_{ca}} \begin{bmatrix}S_{b+}\\S_{a-}\end{bmatrix} \xRightarrow{-v_{ca}} \begin{bmatrix}S_{b+}\\S_{c-}\end{bmatrix}$

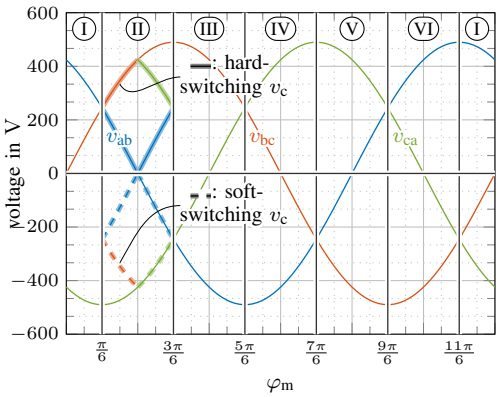


Fig. 4. Ideal line-to-line voltage waveforms at unity power factor. For sector (II), the switching voltages for the respective commutation sequence is displayed according to **Tab. I**. Solid bold lines indicate hard-switching events in sector (II) whereas dashed lines indicate soft-switching events.

- MODE 1: Constant DC-link current. Varying the output current is achieved by changing the modulation index.
- MODE 2: Constant modulation index of $M = 1$. Varying the output current is achieved by controlling the DC-link current accordingly.
- MODE 3: 2/3 modulation [14], [15]. The DC-link current is modulated to operate the inverter stage at the outer boundary of the CSI hexagon in **Fig. 2** decreasing the number of switching transitions per PWM period.

A detailed description of the operating modes can be found in the subsequent sections.

It is important to note that these modes focus exclusively on the efficiency and operation of the inverter stage. The input stage can be replaced with various alternative topologies, such as a multilevel buck-stage to mitigate common-mode EMI in a DC-AC system or a three-phase PWM current source rectifier for an AC-AC system. The only requirement for the input stage is its ability to control the DC-link current within a specified range to facilitate the proposed modes of operation. In the present work, a two-level buck-stage is used for the subsequent practical investigation of the different modes. For the purpose of this comparison, it is assumed that the inverter stage operates at unity power factor, produces sinusoidal output currents free of harmonics, and that the DC-link current shows no ripple.

A. MODE 1: Constant DC-Link Current

In the first mode, the DC-link current i_{dc} of the inverter system is maintained constant by the input buck-stage. The amplitude of the three-phase output current is varied by adjusting the length of the reference space vector $\underline{m}$, referred to as the modulation index M hereafter. The expected three-phase output currents (i_a, i_b, i_c) during a load-step in this mode are shown in **Fig. 5**.

As the DC-link current continuously flows through four semiconductor switches (two active switches and two reverse-blocking devices), the conduction losses P_c for MODE 1 can be calculated by

$$P_c^{\langle 1\rangle} = 4 \cdot R_{ds(on)} \cdot \bar{i}_{dc\,max}^2. \tag{2}$$

Here, $R_{ds(on)}$ represents the on-resistance of the devices, and $\bar{i}_{dc\,max}$ denotes the maximum occurring average DC-link current, based on the inverter's nominal output current. The computation of the switching losses utilizes the linear loss model derived in Section III. According to the switching scheme presented in **Tab. I** (MFSM), for sector (II) where $v_{ab} > 0$ ($\varphi_m = \frac{pi}{6} \ldots \frac{2\pi}{6}$ for unity power factor), the commutation current remains positive throughout the sector as switching operations only take place between the three upper switches S_{a+}, S_{b+}, and S_{c+}. This results in two hard-switching transitions involving v_{ab} and v_{bc}, and two soft-switching commutations with $-v_{ab}$ and $-v_{bc}$. The switching losses for this commutation sequence can therefore be calculated using (3).

$$\begin{aligned} P_s^{\langle 1\rangle} = \frac{f_{pwm}}{\frac{\pi}{6}} \cdot \int_{\frac{\pi}{6}}^{\frac{2\pi}{6}} & E_{soft}(-v_{ab}, \bar{i}_{dc\,max}) \\ & + E_{soft}(-v_{bc}, \bar{i}_{dc\,max}) \\ & + E_{hard}(v_{ab}, \bar{i}_{dc\,max}) \\ & + E_{hard}(v_{bc}, i_{dc})\,\mathrm{d}\varphi \\ = \frac{3\sqrt{3}\,f_{pwm}}{\pi} & \cdot (k_{hard} + k_{soft}) \cdot \bar{i}_{dc\,max} \cdot \sqrt{2}\,V_{ac} \end{aligned} \tag{3}$$

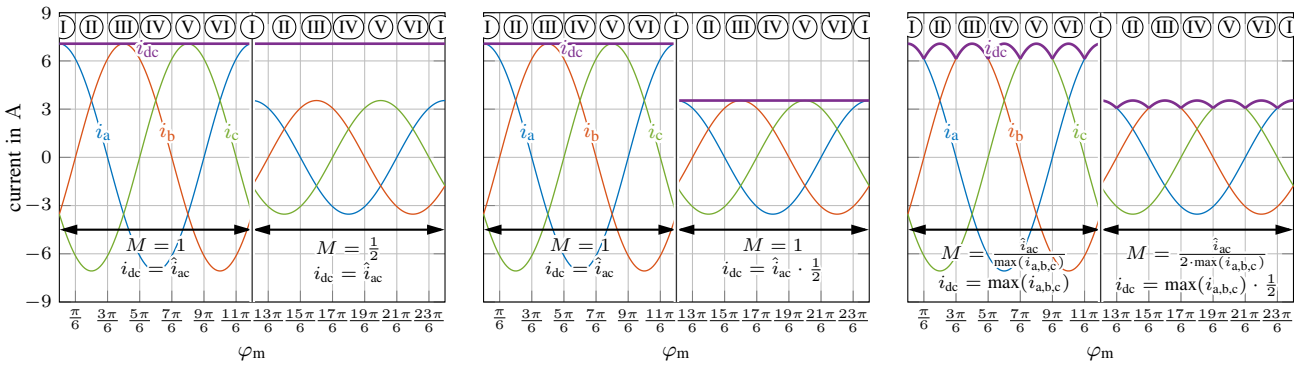
Here, f_{pwm} denotes the PWM switching frequency, and k_{hard} and k_{soft} are the constants for hard- and soft-switching, respectively, from the proposed switching loss model in Section III. $\bar{i}_{dc\,max}$, again, the maximum occurring average DC-link current, and V_{ac} is the RMS value of the output phase voltage.

In **Fig. 6a** the calculated converter efficiency $\eta^{\langle 1\rangle}$ in MODE 1 at unity power factor, and a arbitrarily chosen $k_{soft} + k_{hard} = 50\,\mu J$, $R_{ds(on)} = 100\,m\Omega$, and $f_{pwm} = 100\,kHz$ is given for the whole RMS output voltage and current range (V_{ac}, I_{ac}). The efficiency is calculated by $\eta = \frac{P_{ac}}{P_s + P_c + P_{ac}}$ where P_{ac} denotes the converter output power on its AC side.

B. MODE 2: Variable DC-link Current

As the buck-stage at the converter input is able (or required) to control the DC-link current to a desired value, it is possible to operate the inverter stage at a modulation index of $M = 1$ and adjust the three-phase output current amplitude by varying the DC-link current instead. In case of a grid connected CSI the rectifier stage is in charge to control the DC-link current. This approach allows for a reduction in the DC-link current magnitude during partial load operation, significantly decreasing the conduction losses in the semiconductor switches and the DC-link inductor.

The conduction losses $P_c^{\langle 2\rangle}$ and switching losses $P_s^{\langle 2\rangle}$ in MODE 2 can be computed using (2) and (3), however for the second mode $\bar{i}_{dc}$ is not constant anymore and changes based on the required output current ($\bar{i}_{dc} = \hat{i}_{ac}$).



(a) **(b)** **(c)**

Fig. 5. Idealized curves of the three-phase output current with a load step from maximum current to half of the maximum current. **(a)** Operating MODE 1: DC-link current is constant and current amplitude is adjusted using modulation index M. **(b)** Operating MODE 2: DC-link current is adjusted accordingly and M is kept constant. **(c)** Operating MODE 3: 2/3 PWM modulation.

The calculated efficiency curve for this mode, $\eta^{\langle 2 \rangle}$ is shown in **Fig. 6**. It is observed that for the load condition where maximum power is achieved, the efficiency remains constant across the entire output current range, rather than decreasing at lower operating power levels.

C. MODE 3: Modulation of DC-link current

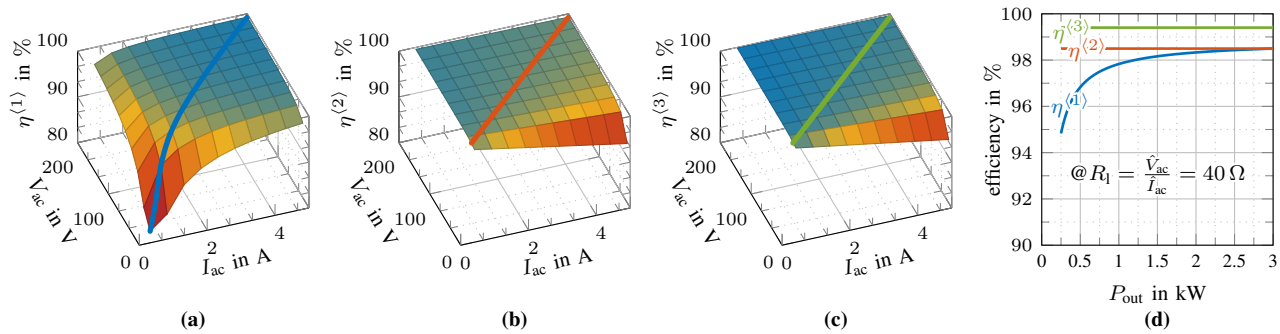
The third mode involves not only varying the DC-link current to adjust the output current amplitude at a constant modulation index but also modulating it advantageously within each period of the three-phase output current to optimize conditions for space vector modulation (SVM). This method has already been discussed in [14], [15] and is referred to as 2/3 modulation. In this approach, the DC-link current i_{dc} is modulated in such a way that only two active space vectors during each PWM period are required to achieve sinusoidal output quantities and the zero, or freewheeling states can be skipped.

The operating principle for this mode is as follows: As described in Section II, a locally averaged current $\underline{i}^*$ is generated using space vector modulation (SVM). When $\underline{m}$ operates precisely at the border of the SVM hexagon, only the two space vectors that bound the sector of the reference space vector $\underline{m}$ are needed to synthesize the desired current. However, as the reference space vector no longer traces a circular path, the DC-link current must be modulated to follow the peak values of the three-phase AC currents ($i_{dc} = \max(i_a, i_b, i_c)$) in order to avoid distorting the sinusoidal output current waveforms. This modulation strategy results in the DC-link current waveform shown in **Fig. 5c**. The resulting switching transitions for this state are listed in **Tab. I**. As the DC-link current is modulated to maintain sinusoidal output quantities, the conduction losses are reduced compared to those in MODE 1. These losses can be calculated using (4).

$$\begin{aligned} P_c^{\langle 3 \rangle} &= 4 \cdot R_{ds(on)} \cdot \frac{3}{\pi} \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} \hat{i}_{dc}^2 \cdot \cos(\varphi)^2 \, d\varphi \\ &= 4 \cdot R_{ds(on)} \cdot \hat{i}_{dc}^2 \cdot \frac{3\sqrt{3} + 2\pi}{4\pi} \end{aligned} \tag{4}$$

The DC-link current amplitude $\hat{i}_{dc}$ in MODE 3 equals the average DC-link current $\overline{i}_{dc}$ in MODE 2 (compare (2)), therefore, the conduction losses in MODE 3 are reduced to approximately 91 % of the losses observed in MODE 2.

Compared to the previously described MFSM, the 2/3 modulation strategy involves commutation only between phases a and b in sector Ⅱ. Consequently, the equation for the switching losses in (3) can be rewritten to (5), where two of the switching events are excluded. When evaluating the loss model, it is important to note that the



(a) **(b)** **(c)** **(d)**

Fig. 6. Calculated efficiency curves as a function of AC output voltages, V_{ac} and output currents, I_{ac} for the three different modes of operation. **(a)**: Operating MODE 1 where DC-link current is kept constant. **(b)**: Operating MODE 2 where modulation index M is kept constant. **(c)**: Operating MODE 3, 2/3 PWM modulation. **(d)**: Efficiency comparison of all three modes as a function of output power P_{ac} at $R_l = 40\,\Omega$.

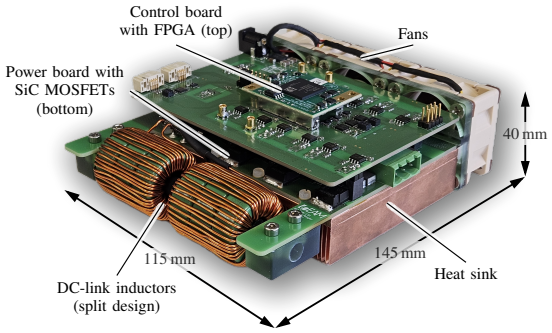


Fig. 7. Implemented buck-CSI prototype featuring a stacked two board design and an integrated thermal management system. The control board containing the driver circuits for the SiC MOSFETs, the ADCs and the FPGA are located on the top board. The SiC MOSFETs with the filter capacitors is located on the bottom board.

DC-link current is no longer constant but instead follows the waveform $i_{\mathrm{dc}} = \hat{i}_{\mathrm{ac}} \cdot \cos\left(\varphi_{\mathrm{m}} - \frac{\pi}{3}\right)$ in sector (II).

$$\begin{aligned} P_{\mathrm{s}}^{\langle 3\rangle} &= \frac{f_{\mathrm{pwm}}}{\frac{\pi}{6}} \cdot \int_{\frac{\pi}{6}}^{\frac{2\pi}{6}} E_{\mathrm{soft}}(-v_{\mathrm{ab}}, i_{\mathrm{dc}}) \\ &\quad + E_{\mathrm{hard}}(v_{\mathrm{ab}}, i_{\mathrm{dc}})\,\mathrm{d}\varphi \\ &= \frac{3\sqrt{3}\,f_{\mathrm{pwm}}}{4\,\pi} \cdot (k_{\mathrm{hard}} + k_{\mathrm{soft}}) \cdot \hat{i}_{\mathrm{dc}} \cdot \sqrt{2}\,V_{\mathrm{ac}} \end{aligned} \tag{5}$$

The resulting switching losses at unity power factor for the 2/3 modulation are $1/4$ of those for the MFSM. The corresponding efficiency curve $\eta^{\langle 3\rangle}$ is also shown in **Fig. 6c**.

V. Experimental Verification

The three proposed modes of operation for the CSI are experimentally verified using a current-source converter laboratory prototype. It consists of a three-phase CSI output stage for motor drives and includes a buck input stage for operation from a DC voltage source, such as a battery or a fuel cell, as described in the basic circuit diagram in **Fig. 1**.

A photograph of the developed prototype is shown in **Fig. 7**. The nominal AC output power of the converter is $P_{\mathrm{ac}} = 3\,\mathrm{kW}$, at a maximum RMS output voltage of $V_{\mathrm{ac}} = 200\,\mathrm{V}$, resulting in a maximal DC-link current of $\bar{i}_{\mathrm{dc\,max}} = 7\,\mathrm{A}$. The maximum DC input voltage of the system is $V_{\mathrm{dc}} = 500\,\mathrm{V}$. The initial PWM carrier frequency was chosen to be $f_{\mathrm{pwm}} = 100\,\mathrm{kHz}$ for both the buck-stage and the CSI, although it was possible to increase this frequency to 200 kHz for the inverter-stage as well as the buck-stage. Experimental tests show that the inverter stage can be operated with switching frequencies of up to 400 kHz, however the buck-stage can only be operated at a maximum of 200 kHz due to increased switching losses. Please note that for all experiments, the buck stage (if operational) was operated in closed-loop control, while the inverter stage was operated in open-loop control.

The laboratory prototype includes an FPGA-based control platform running a custom control scheme, on-board ADCs, and an integrated thermal management system for the power semiconductor switches consisting of a copper heat-sink and three axial fans. The reverse voltage blocking capability of the main switching elements was achieved using a common source back-to-back configuration of two SiC based MOSFETs (IMBG65R072M1H) in a small footprint SMD package (TO-263-7). For the DC-link inductor L_{dc}, a split toroidal inductor was designed according to [16] and implemented, as shown in **Fig. 1**. The filter capacitors are ceramic capacitors based on C0G material that are placed as close as possible to the semiconductor switches, further minimizing the area of the commutation loop and decreasing switching losses. **Tab. II** provides a detailed summary of the prototype specification.

Table II
Summary of the Prototype Specifications

Parameter	Symbol	Value
Nominal output power	P_{ac}	3 kW
Nominal output voltage	V_{ac}	200 V
Nominal output current	I_{ac}	5 A
DC-link current	$\bar{i}_{\mathrm{dc}}$	7 A
Design switching frequency	f_{pwm}	100 kHz
DC-link inductance	L_{dc}	1158 µH
Filter capacitance	C_{f}	800 nF
Power semiconductor	-	IMBG65R072M1H
CSI overlap time	t_{ol}	30 ns
buck-stage interlock time	t_{il}	50 ns

A. Experimental Results

The theoretical findings from Section IV were experimentally verified by the implemented prototype. Therefore, efficiency measurements were conducted over the whole nominal load range of the converter.

For the first set of experiments the buck-stage of the inverter was not in operation meaning the upper switch $S_{\mathrm{HB+}}$ was constantly turned-on and the CSI stage (including the DC-link) was supplied directly via a constant current power supply. The circuit was loaded by a three-phase resistive load of $R_{\mathrm{l}} = 40\,\Omega$ per phase resulting in the transmission of the nominal output power P_{ac} at modulation index $M = 1$ and a nominal average DC-link current of $\bar{i}_{\mathrm{dc\,r}} = 7\,\mathrm{A}$. In this mode losses occur in the inverter stage (conduction and switching losses), the DC-link inductor and $S_{\mathrm{HB+}}$ (conduction losses). As it is not possible to modulate the DC-link current by the power supply, only operating MODE 1 and MODE 2 can be verified in this case. The curves $\eta^{\langle 1\rangle}$ and $\eta^{\langle 2\rangle}$ in **Fig. 8a** and **Fig. 8c** show the measured efficiency (Yokogawa WT5000) of the CSI stage (including the aforementioned additional losses) for inverter switching frequencies of 100 kHz and 200 kHz, respectively. Both operating mode achieve the same inverter stage efficiency of 98.6 % at 100 kHz and 98.3 % at 200 kHz at nominal power. The partial load behavior resembles the expected outcomes derived in Section IV, with $\eta^{\langle 2\rangle}$ remaining almost constant ($\eta^{\langle 2\rangle} \sim 98.6\,\%$ at 100 kHz and $\eta^{\langle 2\rangle} \sim 98.3\,\%$ at 200 kHz) across the entire load range and $\eta^{\langle 2\rangle}$ decreasing sharply towards lighter loads. This results in

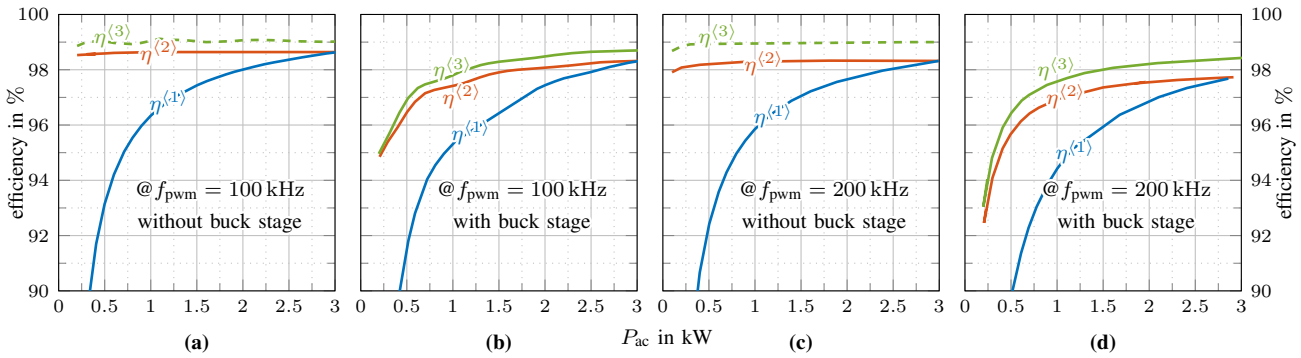


Fig. 8. Measured efficiency (Yokogawa WT5000) of the implemented converter for the three different operating modes. **(a)**: Directly measured efficiency curves $\eta^{\langle 1\rangle}$ and $\eta^{\langle 2\rangle}$ for operation in MODE 1 and 2 at $f_{\text{pwm}} = 100\,\text{kHz}$, with the buck-stage not in operation. The efficiency $\eta^{\langle 3\rangle}$ of the inverter stage in MODE 3 is estimated from measurements taken with the buck-stage in operation and a resistive load $R_{\text{l}} = 40\,\Omega$. **(b)**: Efficiency measurements of the full converter system (including the buck-stage) operating from a 500 V supply for all three modes at $f_{\text{pwm}} = 100\,\text{kHz}$. **(c)** and **(d)**: Measured curves as in the previous plots at $f_{\text{pwm}} = 200\,\text{kHz}$.

poor low-load efficiency for both investigated switching frequencies. Measured voltage and current waveforms (Tektronix 5 Series, measurement bandwidth 50 MHz) for MODE 1 and MODE 2 at $f_{\text{pwm}} = 100\,\text{kHz}$ and $P_{\text{ac}} = 2\,\text{kW}$ ($R_{\text{l}} = 40\,\Omega$) are provided in **Fig. 9a** and **Fig. 9b**. In **Fig. 9a** The DC-link current in is kept constant at 7 A and the modulation index M is adjusted to achieve the desired output current amplitude. In **Fig. 9b**, the same amplitude is achieved by lowering the DC-link current to 5.8 A and maintaining $M = 1$.

For the second set of experiments, the buck-stage was put in to operation to control the DC-link current and provide power from a DC power supply with a DC-voltage of 500 V. Again, the efficiency of the converter system was measured for all three proposed modes of operation. The measured total converter efficiency is shown in **Fig. 8**, where **Fig. 8b** shows the efficiency curves for all three operating modes at $f_{\text{pwm}} = 100\,\text{kHz}$ and **Fig. 8d** at $f_{\text{pwm}} = 200\,\text{kHz}$. In contrast to the results without buck-stage the efficiencies $\eta^{\langle 1\rangle}$ and $\eta^{\langle 2\rangle}$ are smaller than the ones without the buck-stage in operation and experience a strong decline towards lighter load conditions for both tested switching frequencies while the now acquired $\eta^{\langle 3\rangle}$ in operating MODE 3 provides the highest efficiency. In **Fig. 9c** the measured inverter voltages and currents for operating MODE 3 are given for $f_{\text{pwm}} = 100\,\text{kHz}$, and $P_{\text{ac}} = 2\,\text{kW}$. Here the introduced ripple by the buck-stage can be observed in the DC-link current waveform.

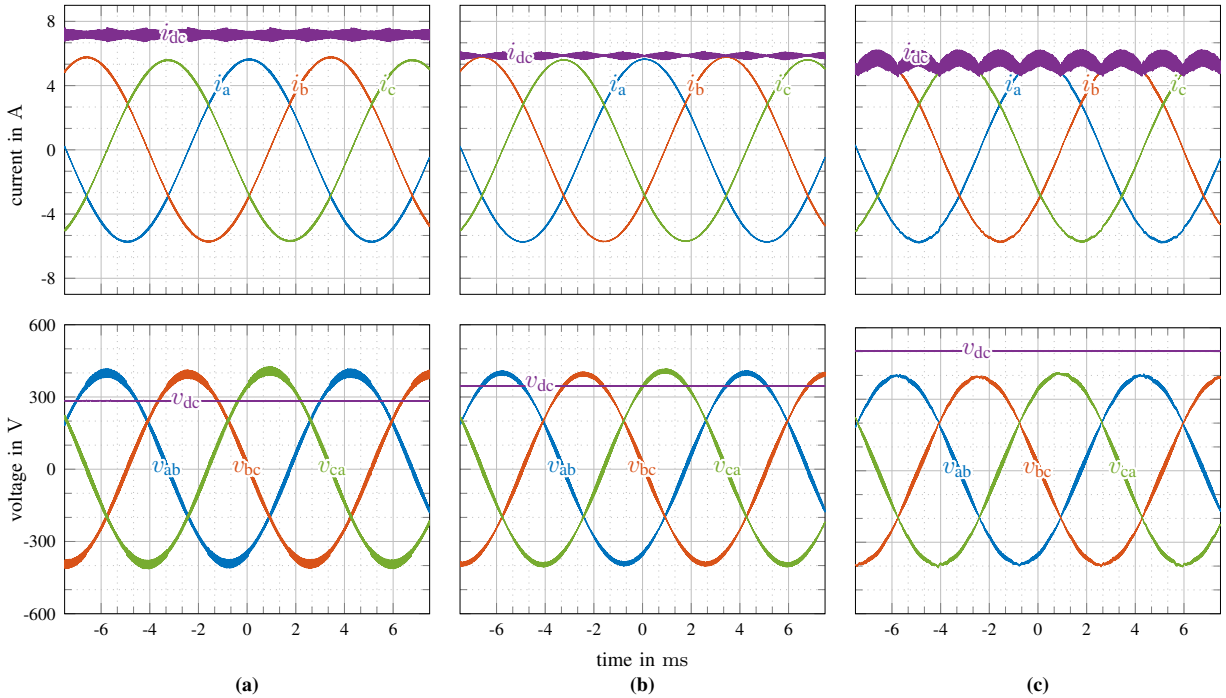


Fig. 9. Measured voltage and current waveforms (Tektronix 5 Series, measurement bandwidth 50 MHz) each for a different mode of operation at a PWM Switching frequency $f_{\text{pwm}} = 100\,\text{kHz}$ and output Power $P_{\text{ac}} = 2\,\text{kW}$ and restive load of $R_{\text{l}} = 40\,\Omega$ per phase ($\hat{\imath}_{\text{ac}} \sim 5.8\,\text{A}$). **(a)**: Operating MODE 1 and **(b)** operating MODE 2 where in both operating modes the buck-stage was not in operation. **(c)**: Operating MODE 3 (2/3 PWM) with buck-stage in operation.

Based on these measurements, the efficiency of only the inverter stage for operating MODE 3 can be estimated for comparison with the other two operation modes. As it is not possible to directly measure the inverter losses with a power analyzer while the buck-stage is operational, it is feasible to estimate the efficiency of the inverter stage for MODE 3. This estimation allows for a comparison with the efficiencies of the other two modes. The buck-stage losses for MODE 3 and MODE 1 are very similar, given the comparable average input voltage and DC-link current levels. Therefore, the measured losses in operating MODE 1 without the buck-stage are subtracted from the measured losses in MODE 2 with the buck-stage in operation to obtain an estimate for the buck-stage losses.

$$P_{\text{buck}}^{\langle 1,3\rangle} \approx P_{\text{loss nobuck}}^{\langle 1\rangle} - P_{\text{loss buck}}^{\langle 1\rangle} \tag{6}$$

Where the losses are the difference between measured DC- and AC side power ($P_{\text{loss}} = P_{\text{dc}} - P_{\text{ac}}$). These buck-stage losses are subtracted from the measured losses in MODE 3.

$$P_{\text{loss nobuck}}^{\langle 3\rangle} \approx P_{\text{loss buck}}^{\langle 3\rangle} - P_{\text{buck}}^{\langle 1,3\rangle} \tag{7}$$

The resulting efficiency curves for $\eta^{\langle 3\rangle}$ are displayed additionally in **Fig. 8a** and **Fig. 8c** for $f_{\text{pwm}} = 100\,\text{kHz}$ and $f_{\text{pwm}} = 200\,\text{kHz}$. They reassemble the expected behaviour derived in Section IV being almost constant across the whole load range and higher than the measured efficiency in MODE 1. In addition, the losses are only slightly reduced when the switching frequency is increased ($99\,\%$ to $98.9\,\%$ from $100\,\text{kHz}$ to $200\,\text{kHz}$ at $P_{\text{ac}} = 2\,\text{kW}$), as the conduction losses in the switches and the DC-link inductor dominate due to the reduced number of switching operations

VI. Conclusion

This paper presented an analytical and experimental benchmark of three different modulation schemes for the buck-CSI. In addition to the efficiency improvements achievable in MODE 1 and MODE 2 (2/3 modulation), the paper highlights the stable inverter performance at increasing switching frequencies. This feature can be further exploited in converter design to achieve an optimal trade-off between efficiency and power density, depending on specific application requirements.

Given the limited applicability of 2/3 modulation to voltage boosting regimes, as required by high rotational speeds and/or high-pole number machine designs, the results suggest that a hybrid modulation scheme combining operation MODE 2 and 2/3 modulation could be an effective way to optimize performance across a broad range of operational conditions.

Future work will focus on further increasing the switching frequency of the presented current-source converter system. A switching frequency of $400\,\text{kHz}$ has already been achieved for the inverter stage in MODE 1 and 2, however the buck-stage switching frequency can't exceed $200\,\text{kHz}$ due to excessive losses.

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