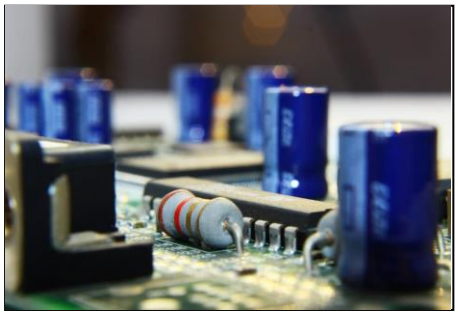
Institut für Elektronik

Master's thesis

In cooperation with amsAG

Digital Design - Low Power Digital Design Flow using IEEE-1801 UPF



Current Status and Motivation:

Low power design and verification are increasingly necessary in today's IC design.

The IEEE 1801 standard, Unified Power Format (UPF), is an industry wide power format specification to enable low power design and verification from RTL verification through physical design and implementation.

This master thesis will evaluate UPF-based low power design, verification, and implementation based on ams CMOS technology using EDA (Electronic Design Automation) tools available at ams AG.

Research Topic(s):

Evaluate Digital Design Tools and acquire skills in UPF Methodology. Review different CMOS technologies for power optimization capabilities. Combine these disciplines to a low power design flow.

Approach / Methodology:

- Introduction to UPF
- Generate multi power demo design & review example design – HDL design
- UPF @ digital frontend, digital backend and design verification – implementation
- UPF design flow, methodology – documentation

Basic experience in Verilog HDL and EDA tools (simulation, synthesis, PnR) is an advantage

Organisational Matters:

- Start of work: Q2 2021
- Workplace: Premstätten (ams AG)
- Paid thesis: x k€
- Text

Contact person / Supervisor:

IFE: Prof. Bernd Deutschmann, bernd.deutschmann@tugraz.at
Company: DI Bodo Kaufmann, bodo.kaufmann@ams.com, 0677 61395819